APPLICATION FOR UNITED STATES LETTERS PATENT
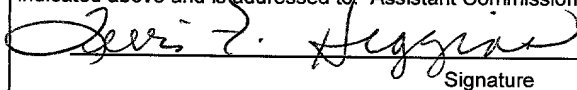
for

UNINTERRUPTIBLE POWER SUPPLY

by

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H 457948(9TCS01! DOC)

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application serial number 60/244,005, filed October 27, 2000.

BACKGROUND OF THE INVENTION

The present invention relates to uninterruptible power supplies, and, in particular, the control of uninterruptible power supplies. Historically, uninterruptible power supplies have relied on traditional analog control techniques, which are limiting in the level of control that can be provided and in the aspects of the uninterruptible power supply's operation that can be controlled. Accordingly, what is needed in the art is an uninterruptible power supply featuring digital control, which allows greater flexibility and more precise control of the uninterruptible power supply.

SUMMARY OF THE INVENTION

In one aspect the present invention is directed to an uninterruptible power supply comprising a controlled rectifier a battery an inverter and a control system. The control system is coupled to the controlled rectifier and the inverter, as well as other uninterruptible power supply components. The control system comprises three microprocessors, with the first microprocessor functioning as an overall controller, the second microprocessor controlling the rectifier, and the third microprocessor controlling the inverter. In another aspect of the invention, the three microprocessors communicate via a common global memory. This common global memory is facilitated by a memory arbitration circuit that allows priority-driven, non-preemptive access by the microprocessors to the common global memory.

In another aspect of the present invention, the various components of the UPS are connected by a peer-to-peer controller area network that accommodates fragmented messaging.

In still another aspect of the present invention the uninterruptible power supply includes a battery monitoring circuit that allows a single sensor to be used despite the wide disparity in dynamic range between the battery charging current and the battery discharging current. The battery monitoring circuit includes a current sensor disposed to monitor the battery current, with a first amplifier circuit receiving an output from the current sensor corresponding to discharging battery current and a second amplifier circuit

1   receiving an output from the current sensor corresponding to a charging battery current.

2   The two amplifier circuits amplifying the received current signal by a relatively smaller

3   factor for the relatively larger discharging current and by a relatively larger factor for the

4   relatively smaller charging current respectively. The digital control system then selects

5   the appropriate amplifier's output as its input depending upon whether the battery is

6   charging or discharging.

7   In yet another aspect of the present invention, the digitally controlled UPS having

8   a three-phase input features independent zero-crossing detection circuits for each input

9   phase. The zero-crossing detection circuits are used to synchronize the firing of the

10 controlled rectifier to the input voltage. The rectifier control microprocessor

11 independently determines a phase shift introduced by each zero cross detection circuit

12 and adjusts the firing signal timing for each rectifier phase to negate the phase shift.

13   Still another aspect of the present invention allows the second microprocessor of

14 the uninterruptible power supply to change the firing sequence of the rectifier to

15 compensate for a phase rotation of the three-phase input. In yet another aspect of the

16 present invention, the second microprocessor qualifies the input voltage by measuring the

17 voltage on a first phase of said three-phase input, the frequency on a second phase of said

18 three-phase input, and the phase sequence between either said first phase or said second

19 phase and a third phase of said three-phase input. In another aspect of the present

20 invention the second microprocessor implements a phase lock loop for synchronizing

21 rectifier firing. The phase lock loop includes a finite impulse response filter on the input

22 voltages, thereby removing low frequency harmonics from the input signal.

23   In another aspect of the invention relating to control of the inverter, the third

24 microprocessor implements a nested control loop having an inner loop and outer loop.

25 The inner loop regulates inverter current using a discrete sliding mode controller, and the

26 outer loop regulates the inverter voltage using a harmonic servomechanism controller.

27   In another aspect of the invention relating to control of the rectifier, there is a

28 method of controlling the output of the controlled rectifier. The method includes, sensing

29 the voltage on the DC bus at the rectifier's output, comparing the sensed voltage to a

30 voltage setpoint, increasing or decreasing the rectifier firing angle to minimize a

31 difference between the sensed voltage and the voltage setpoint, and determining whether

an input current of the rectifier or a charging current of the battery is above a predetermined limit; and, if so, switching control to a different control loop to maintain the input current or the charging current within the predetermined limit. In implementing this method, it is beneficial to pre-load the integrator of the different control loop when switching to a different control loop to prevent a discontinuity in an output signal of the different control loop. It is also advantageous to include a non-linear element in the control loop to improve the response to a step change in the applied load.

In another aspect of controlling the rectifier, it is also advantageous to gradually increase the voltage setpoint on startup to softly start the rectifier and avoid undesirable startup transients. Additionally, the voltage setpoint is selected to cause a particular charging current to flow into said battery, and the setpoint may be selected from a plurality of different values to vary the charging rate. The voltage setpoint may selected to cause zero charging current to flow into said battery. Finally, voltage setpoint may be selected as a function of battery temperature.

In still another aspect of the present invention, a technique is disclosed for operating a plurality of uninterruptible power supplies in parallel. The method includes controlling real power sharing between the uninterruptible power supplies by adjusting the relative phase angles of the generated voltages. Reactive power sharing is achieved by relative adjustment of the amplitude of the voltage generated by each uninterruptible power supply. Harmonic current sharing among the uninterruptible power supplies is achieved by shifting the poles of the harmonic controller to reduce the bandwidth for the controller corresponding to the harmonic, thereby increasing the impedance to that harmonic.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an uninterruptible power supply in accordance with the present invention.

Fig. 2 is an expanded block diagram of an uninterruptible power supply in accordance with the present invention

Fig. 3 is an expanded block diagram of an uninterruptible power supply and uninterruptible power supply control system in accordance with the present invention.

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Fig. 4 is a block diagram of the Micro Monitor uninterruptible power supply interface system.

Fig. 5 is a schematic diagram of the rectifier/charger and controller therefor used in the uninterruptible power supply of the present invention.

Fig. 6 is a schematic diagram of the static switch and controller therefor used in the uninterruptible power supply of the present invention.

Fig. 7 is a block diagram of the uninterruptible power supply of the present invention showing sensor locations and connections.

Fig. 8 is a flow chart illustrating the static switch contactor startup process used in the uninterruptible power supply of the present invention.

Fig. 8a is a flow chart illustrating the DSP startup sequence used in the uninterruptible power supply of the present invention.

Fig. 9 is a flow chart illustrating the static switch startup process used in the uninterruptible power supply of the present invention.

Fig. 10 is a flow chart illustrating the input contactor startup process used in the uninterruptible power supply of the present invention.

Fig. 11 is a flow chart showing the rectifier startup process used in the uninterruptible power supply of the present invention.

Fig. 12 is a flow chart showing the input filter startup process used in the uninterruptible power supply of the present invention.

Fig. 13 is not used.

Fig. 14 is a flow chart showing the battery startup process used in the uninterruptible power supply of the present invention.

Fig. 15 is a flow chart illustrating the inverter startup process used in the uninterruptible power supply of the present invention.

Fig. 16 is a diagram illustrating operation of the software-implemented, digital phase locked loop used in the uninterruptible power supply of the present invention.

Fig. 17A-B is a block diagram of the rectifier control system used in the uninterruptible power supply of the present invention.

Fig. 18A-C is a schematic diagram of the transistor saturation detection circuitry disclosed in the disclosed uninterruptible power supply.

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Fig. 19 is a simplified schematic of an inverter for use in a UPS according to the present invention.

Fig. 20 is a table illustrating the inverter switching states and corresponding output voltages for the inverter illustrated in Fig. 19.

Fig. 21 is a voltage vector diagram showing the possible output voltage vectors of the inverter shown in Fig. 19.

Fig. 22-22A illustrates the generation of inverter voltages using the space vector PWM technique.

Fig. 23 is a sample overload curve for an uninterruptible power supply.

Fig. 24 is an equivalent energy curve corresponding to the overload curve illustrated in Fig. 23.

Fig. 25 is a schematic diagram of a battery current measurement circuit used in the disclosed UPS.

Fig. 26 is a block simplified block diagram of the UPS illustrating the control parameters used to design the control system.

Fig. 27 is a simplified block diagram of the UPS control system.

Fig. 28 is an expanded block diagram of the UPS control system.

Fig. 29 is a timing diagram illustrating the look-ahead prediction employed by the controller.

Fig. 30 is a simplified schematic of the UPS illustrating the control variables used in controlling the UPS.

Fig. 31 is a schematic of the equivalent circuit of the output transformer illustrating the control variables.

Fig. 32 is a first portion of an expanded block diagram illustrating the harmonic servo compensator used in the UPS of the present invention.

Fig. 33 is a second portion of an expanded block diagram illustrating the harmonic servo compensator used in the UPS of the present invention.

Fig. 34 is not used.

Fig. 35 is a schematic diagram of the memory arbitrator circuit employed in the UPS of the present invention.

1 Fig. 36 is a communication diagram for a successful fragmented message

2 transmission.

3 Fig. 37 is a communication diagram for the receipt of a fragmented message when

4 the receiver is busy.

5 Fig. 38 is a schematic diagram of the rectifier firing pulse generation/control

6 circuit.

DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

8 I. UPS TOPOLOGY

9 An uninterruptible power supply ("UPS") in accordance with the present

10 invention is illustrated in Fig. 1. The UPS includes the rectifier/charger 2, battery 3, DC

11 bus 10, inverter 4, bypass switch 5, control module 7, and output transformer 13. Under

12 normal operating conditions, alternating current ("AC") power is supplied at the input 1.

13 The AC power follows the first power path 9 to the rectifier/charger 2. The

14 rectifier/charger 2 converts the incoming AC voltage to a direct current ("DC") voltage.

15 This DC voltage is supplied to battery 3 to charge the battery. The DC voltage is also

16 supplied to the DC bus 10, which powers inverter 4. Inverter 4 converts the supplied DC

17 voltage to an AC voltage that is then supplied to the load 6 via the output transformer 13.

18 If one of the UPS components fails or if the UPS power rating is insufficient to

19 power load 6, power flows from the input 1, along a second power path 8, to bypass

20 switch 5. Bypass switch 5 is closed, enabling power flow directly from input 1 to load 6

21 via the output transformer 13. If the normal AC power source fails, battery 3 provides

22 power to the DC bus 10. Inverter 4 takes DC power from bus 10, converts it to AC

23 power, and supplies it to the load 6 via the output transformer 13.

24 Control system 7 controls the rectifier/charger 2, inverter 4, and bypass switch 5.

25 Control system 7 monitors the input and output voltages and currents and controls the

26 rectifier to charge the battery and regulate the DC bus voltage. The control system is

27 discussed in greater detail below.

28 A preferred embodiment of the UPS of the present invention is illustrated in Fig.

29 2. Input filter 11 has been inserted along first power path 9 before rectifier/charger 2.

30 This input filter reduces the THD of the AC power supplied at input 1. Input filter 11 is a

31 10% harmonic trap filter. The design construction of such filters is known to those

skilled in the art. The filter includes a three-phase input filter inductor. The first terminals of said inductor are connected to the AC input lines, and the second terminals are connected in parallel with a trap inductor and a trap capacitor connected in a second order low pass LC filter arrangement. The output of input filter 11 is connected to the input of rectifier/charger 2.

The preferred UPS embodiment shown in Figure 2 further includes an output LC filter 12 connected to the output of inverter 4. This output filter reduces the distortion of the power waveform supplied to load 6. Output LC filter 12 is a three-phase, second order LC filter that eliminates high frequencies from the voltage generated by inverter 4. Construction and implementation of such filters is well known in the art.

The preferred UPS embodiment further includes an isolation transformer 13 connected at the output of LC filter 12. This transformer provides electrical isolation between critical load 6 and the UPS. Isolation transformer 13 is preferably a three-winding delta-wye isolation transformer, but other transformer designs may also be used.

An output filter 14 is also included in the preferred UPS embodiment illustrated in Fig. 2. This output filter serves to further reduce distortion in the voltage waveform at the output of isolation transformer 13. Output filter 14 is preferably a three-phase capacitor connected across output windings of isolation transformer 13. The capacitor in combination with the leakage inductance of the transformer operates as a second order low pass filter. The output of filter 14 is connected between isolation transformer 13 and load 6.

Major components of the UPS will now be discussed in greater detail.

A. Power Circuitry

1. Rectifier

Rectifier/charger 2 is a phase fired, six-pulse rectifier. The rectifier comprises three pair of series connected SCRs, i.e., a six-pulse rectifier. Optionally, the UPS of the present invention may include a twelve-pulse rectifier. Use of a twelve-pulse rectifier design improves the total harmonic distortion ("THD") reflected back on the AC input lines. Those skilled in the art are familiar with the design and implementation of such rectifiers. The purposes of the rectifier are to provide a stable DC bus and to maintain the battery's charge.

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All rectifier control is accomplished by controlling the firing angle of the rectifier SCRs. The required phase information is derived using a digitally-implemented zero cross detector. An alternate method of deriving the phase information is by use of a digitally implemented phase lock loop (PLL). In either case, each phase of the rectifier is controlled independently. Both of these methods are discussed in greater detail below.

Control of the rectifier firing angle controls the DC bus voltage under the direction of control system 7. The rectifier controls the incoming AC current to produce an acceptable voltage on the DC bus 10, provided that the AC input voltage is at least -20% and less than +15% of the nominal AC voltage. If the supplied AC voltage is outside this range, power is drawn from the battery to make up the difference between the output power and input power. If the incoming line voltage decreases below the acceptable tolerance, the control system increases the firing angle of the SCRs to draw the maximum possible power from the incoming AC line. The control system will continue to increase the SCR firing angle until the incoming line current reaches the rectifier input current limit or the firing angle is fully on.

On startup, the rectifier controls the DC bus voltage in a technique known as battery walk-in. Battery walk-in is used to prevent transient battery currents when the UPS is started. During UPS startup, the DC bus voltage is lowered to match to the battery voltage. After the battery is connected to the DC bus by closing the battery circuit breaker, the DC bus voltage is slowly increased to begin battery charging.

The rectifier also charges the battery. Charging is controlled by regulating the DC bus voltage, the DC bus voltage being a function of the rectifier firing angle. The battery charging current is directly related to the difference between the DC bus voltage and the battery voltage. By keeping the DC bus voltage relatively constant the battery may be charged with a current that has minimal ripple and other transient components. Eliminating ripple and transients from the battery current prolongs battery life by preventing the negative electrochemical reactions within the battery that are associated with a non-constant charging current.

The rectifier has three different charging modes. A slower ("battery saver") charging mode requires a longer time to fully charge the battery, but prolongs battery life. The battery saver charging mode sets a lower value for the battery current limit, which

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1 has a corresponding lower DC bus voltage. A faster ("turbo") charging mode keeps the
2 battery charged with minimal charging time, but fast charging causes negative
3 electrochemical reactions in the battery that shorten battery life. The faster charging
4 mode sets a higher value for the battery current limit, which corresponds to a higher DC
5 bus voltage. A more detailed discussion of the battery current limit and its effect on DC
6 bus control is discussed below in conjunction with the rectifier control processor.

7   The rectifier may also implement delayed charging. Delayed charging is used
8 when the AC input source has a limited amount of power available, e.g., a standby
9 generator. Prior art UPS systems that charge from the DC bus have typically inhibited
10 charging by using a mechanical contact to isolate the battery from the DC bus. The
11 mechanical contact in such systems is typically actuated by an external source, such as a
12 run indication from a standby generator. In the UPS of the present invention, charging is
13 inhibited by lowering the DC bus voltage to match the battery voltage so that no charging
14 current flows into the battery. The rectifier and inverter are designed so that a DC bus
15 voltage equal to the minimum battery voltage is sufficient for the inverter to deliver full
16 power at full voltage to the critical load. Advantages of this system include providing a
17 reduced number of components that are subject to failure and prolonging battery life by
18 using the walk-in procedure discussed above to slowly change the battery current.

19   Battery charging implemented is also temperature compensated by the control
20 system. As the temperature increases above 25 degrees C, the charging current that can
21 be supplied without damaging the battery decreases. To compensate for temperatures
22 above 25 degrees C, the control system decreases the battery charging current limit,
23 which in turn decreases the DC bus voltage by decreasing the rectifier firing angle.
24 Details of the control system implementation of temperature compensated battery
25 charging are discussed below.

26   2. Inverter

27   Inverter 4 is a three-phase "bridge type" pulse width modulated ("PWM")
28 inverter. Those of skill in the art are familiar with the design and construction of such
29 inverters. Each pole or phase of the inverter is constructed from two series-connected
30 insulated gate bipolar transistors ("IGBTs"). The inverter uses a space vector PWM
31 technique, which will be discussed below.

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1   A simplified schematic diagram of the three phase voltage source inverter used in

2   the UPS of the present invention is illustrated in Fig. 19. A DC input voltage is supplied

3   at the input terminals 101. A three phase output voltage is generated on output terminals

4   108, 109 and 110. The output voltage is generated by switching of transistors 102–107.

5   Transistors 102 and 103 form a totem-pole transistor pair for phase A, transistors 104 and

6   105 form a totem-pole pair for phase B, and transistors 106 and 107 form a totem-pole

7   pair for phase C. The transistors of each totem-pole pair are always in opposite states,

8   e.g., if transistor 102 is on, transistor 103 is off, if transistor 104 is on, transistor 105 is

9   off, etc. Because the transistors operate in complimentary pairs, there are eight possible

10   switching states for the inverter. The eight switching states and corresponding output

11   voltages are illustrated in Fig. 20. The technique for manipulating these switching states

12   to produce the desired output voltage is discussed in greater detail below.

13   3. Bypass Switch

14   Bypass switch 5 is a static switch comprised of six SCRs with contactors at the

15   input and output of the semiconductor switch. Each pole of the static switch is a single

16   back-to-back SCR module comprising two SCRs. Each pair of SCRs is driven by an

17   independent drive circuit on the static switch driver board, discussed below.

18   The bypass switch provides a means to quickly connect the bypass source to the

19   output load. The UPS system can automatically turn on the bypass switch if any

20   abnormal conditions are detected that may jeopardize the quality of the power supplied to

21   the load. The bypass switch can also be turned on and paralleled with the inverter to

22   supplement power to the load in the event of a large transient overload. Furthermore, the

23   bypass switch provides a means to connect an alternate source (bypass source) to the load

24   thus allowing the inverter source to be isolated and disabled for servicing.

25   B. Control Circuitry

26   1. Control Architecture

27   An expanded diagram of the UPS control system 7 is illustrated in Fig. 3. Control

28   system 7 comprises: control board 15; rectifier driver board 16; inverter driver board 17;

29   static switch driver board 18; Micro Monitor user interface 19; voltage current and

30   temperature ("VIT") board 20; high voltage board 21; burden board 22; and general

31   purpose board 23.

a) Control Board

Control board 15 interfaces with Micro Monitor interface 19 to provide a user interface to the UPS. Control board 15 also interfaces with static switch driver 18 to control bypass switch 5. Control board 15 receives measured values required for UPS control from VIT board 20. VIT board 20 receives signals representing the system voltages after they are attenuated by high voltage board 21. The current signals required by control board 15 are supplied to VIT board 20 by burden board 22, which interfaces with the current transformers ("CT") used for AC current measurement at various points in the system. VIT board 20 also receives inputs from general purpose board 23.

Control board 15 is central point control system 7 where all control is performed. Control board 15 includes three digital signal processors ("DSPs") that perform all control computations for the UPS. The first DSP is the Comms DSP 24. The Comms DSP controls high level system functions including monitoring and communications. The second DSP is Rectifier DSP 25. The Rectifier DSP controls rectifier/charger 2. The third DSP is Inverter DSP 26. The Inverter DSP controls inverter 4 and bypass 5. The three processors pass data among themselves through a global random access memory ("RAM"). Details of the global memory management are discussed below.

The Comms DSP also controls high level system functions, including monitoring, and communications. The Comms DSP also performs all metering functions and controls status and alarm signals. The Comms DSP controls the battery circuit breaker and startup/shut down of the UPS. The Comms DSP handles the exchange of status, configuration and diagnostic information externally and internally to the control board. Externally, the Comms DSP exchanges information via a Controller Area Network ("CAN") bus, a service terminal interface and discrete I/O lines. Status and diagnostic information communicated through the UPS includes contactor position sensing, fan operational sensing, fuse status sensing, over temperature sensing, metering data (voltage, current, etc.), control data, and UPS operational status. Control information includes system commands (on, off, transfer, retransfer, etc.), contactor actuation signals, breaker actuation signals, and fan control.

Control system initialization is also performed by the Comms DSP. When the UPS is started, the Comms DSP clears global memory, retrieves system configuration

settings from nonvolatile memory and coordinates system configuration with the Micro Monitor user interface. The configuration information is then relayed to the Rectifier and Inverter DSPs, and the Comms DSP will signal each DSP to start executing the control programs and begin operating the UPS.

The Comms DSP also coordinates systematic shutdown of the UPS. Manual shutdown requests come from the Micro Monitor user interface. In addition to manual actuation, various full or partial shutdown sequences may occur as a result of events or alarms in the UPS. Events that can cause a shutdown include: timing or sanity errors, over temperature, overload, complete battery discharge, and component failures. For a given shutdown sequence, the main objective is to attempt to continue supplying quality power to the load while maintaining a safe operating condition by isolating failed devices or out-of-tolerance system parameters. After shutdown, the Comms DSP tracks status and configuration information to determine whether the machine should be restarted manually by the user (cold start of the machine) or automatically (for example, once AC power is restored after a complete battery discharge).

The Comms DSP also services system level hardware watchdog timer. If the Comms DSP fails to update this watchdog timer within a specified period, the hardware watchdog timer will reset the control board and signal the bypass static switch control board to transfer the load to bypass, thereby preventing critical load interruption.

The Comms DSP also controls a real time clock for the UPS. The real time clock can be set via the service terminal or the Micro Monitor user interface. Time and date information is used for event time-stamping. An event log is kept by the Comms DSP and is stored in nonvolatile memory. A copy of this log may be transferred to the Micro Monitor user interface for review and analysis.

Other logging includes the history log. The history log contains system status information recorded at specified intervals, such as RMS input voltage, output voltage, output current, machine status information, etc. The history log also includes parameters collected for development purposes. Its data represents conditions before, during, and after a fault condition occurs to be used for further analysis of the failure, if necessary. A fast transient analysis (FTA) log may also be stored in non-volatile RAM. The time interval for the FTA log is much shorter than the history log interval time.

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1   The Comms DSP also interfaces to non-volatile RAM for storing configuration

2   data. Configuration data is downloaded to the Comms DSP from the Micro Monitor user

3   interface. This data includes operating set points and ramp rates, derating factors, and

4   system configuration parameters.

5   b)   SCR Driver Board

6   Another component of the UPS control system is the rectifier SCR driver board

7   16. Figure 5 illustrates SCR driver board 16 and its connections to rectifier/charger 2 and

8   control board 15. As noted above, the rectifier is a six-pulse rectifier comprised of six

9   SCRs 34. The input to rectifier/charger 2 comes from the first power path 9 connected to

10   the AC input 1 (not shown). The output of the rectifier connects to DC bus 10, which

11   includes positive DC bus leg 35 and negative DC bus leg 36.

12   SCR driver board 16 has twelve connections to the rectifier/charger 2. Each SCR

13   has its gate and cathode (denoted in the figure) connected to the SCR driver board. SCR

14   driver board 16 also interfaces with control board 15. The connection between the SCR

15   driver board and the control board is by way of sixteen conductor cable 33. The ribbon

16   connector is shrouded, polarized, and has long ejection latches. Gold plated posts are

17   used for improved signal integrity. The connections from the rectifier SCR driver to the

18   SCRs are made via fast-on type terminals. Two of the wires in cable 33 bring 24 VDC

19   power from the control board to the SCR driver board. The remaining connections in

20   cable 33 are the SCR bipolar drive signals. Each SCR has its own independent signal.

21   The control board supplies the SCR controller with 24 VDC power. The SCR driver

22   board includes linear regulating power supplies to derive the +15V and +5V supplies

23   used for SCR control.

24   c)   Inverter Driver Board

25   Turning again to Fig. 3, another UPS control system component is the inverter

26   IGBT driver board 17. The inverter driver board, actually comprises three IGBT driver

27   boards, each of which drives one pole of the three-phase inverter. As noted above, each

28   inverter pole comprises a pair of IGBTs. Each IGBT driver board contains two

29   independent driver circuits, each driving a single IGBT. Each IGBT drive circuit uses an

30   optically isolated driver integrated circuit that meets the regulatory isolation requirements

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1 for a nominal 540 V$_{DC}$ system. The connections between the control board and the

2 inverter driver board are made with 10-wire twisted pair ribbon cables.

3 The three IGBT driver boards interface directly with the control board. The

4 control board provides the necessary control signals and a regulated power supply. The

5 interface to the control board is made via a 10 wire twisted pair ribbon cable. The ribbon

6 cable is terminated with a locking insulation displacement connector with integral strain

7 relief. The mating half of the connector on the IGBT driver board is shrouded header

8 with long locking ears. The connector provides the unregulated control power and driver

9 signals to this board. The IGBT driver board interfaces to the individual IGBT devices

10 via fast-on type terminals.

11 The inverter drive signals from the control board are bipolar drive signals. The

12 drive signal provides 16 mA in both the on and off condition. In the event of a power

13 supply failure, the driver circuit defaults to the off state. The IGBT drive pulse frequency

14 is determined by the switching frequency of the inverter (between 2 kHz and 3 kHz).

15 The IGBT driver board receives its control power from the control board. The

16 control power is a regulated +24 VDC source. The driver board includes an on board

17 DC-DC converter that provides isolated power to the IGBT driver circuits. The on board

18 DC-DC converter operates at approximately 100 kHz to generate +24 VDC that powers

19 the IGBT drives. A control voltage for the logic devices is +5 VDC derived from the +24

20 VDC using a linear regulator. The power requirement for the IGBT board is

21 approximately three watts.

22 d) Static Switch Driver Board

23 Another control system component is the static switch driver board 18. The

24 connection for static switch driver board 18 is illustrated in Figure 6. Input power from

25 AC input 1 branches into two power paths. First power path 9 provides power to

26 rectifier/charger 2. Bypass power path 8 proceeds through "line" bypass contactor 37, to

27 bypass static switch 5 through "load" bypass contactor 38 to isolation transformer 13.

28 Bypass switch 5 is comprised of six SCRs 34. There are two SCRs per phase connected

29 in an anti-parallel configuration. The static switch driver board connects to the gate and

30 cathode of each bypass static switch SCR. Each SCR is simultaneously controlled to

31 permit power flow along the bypass power 8 path if the UPS fails.

1   The static switch control board also controls "line" bypass contactor 37 and

2   "load" bypass contactor 38, which are both closed when the bypass is activated to permit

3   current flow through bypass switch 5.

4   The static switch driver board also interfaces to the micro-monitor interface 19,

5   system switchgear board 39, control power supply 40, and control board 15. The static

6   switch driver board is configured so it will independently transfer the UPS operation to

7   bypass if the control board fails.

8   The static switch driver board is the interface between the control board and the

9   power carrying devices (contactors and SCRs) in the UPS bypass path. Under normal

10   operation the static switch driver board operates the static switch through commands

11   issued by the control board. However, the static switch driver board is also designed to

12   independently transfer the UPS to bypass if the control board malfunctions or fails to

13   communicate with the static switch driver. Under this fault condition the static switch

14   driver board initiates a latched transfer to bypass to prevent power interruption to the

15   load. In the latched bypass mode, the UPS can return to normal operation only after user

16   intervention. The static switch driver logic prevents transfer to bypass if the bypass AC

17   input voltage is outside the acceptable range.

18   The static switch driver board controls three isolated back-to-back SCR modules

19   (six SCRs) located in the internal AC bypass line of the UPS. The static switch driver

20   board includes six isolated drive circuits, each of which controls a single SCR. The gate

21   drive signals are generated from 25% duty factor, 13 kHz internal clock. Pulse

22   transformers in the drive circuits isolate the low voltage logic from the high AC voltage

23   present on the SCRs. Besides driving the SCRs, the static switch driver board also drives

24   the coils of two contactors located on either side of the static switch. These contractors

25   are defined as the "line" and "load" bypass contactors.

26   Besides the control board, the static switch driver board also interfaces with the

27   power supply board, the Micro Monitor user interface and the system switchgear board.

28   Interface to the static switch SCRs is provided via fast-on type terminals. There are

29   twelve fast-on terminals on the static switch driver board to facilitate connection to the

30   three back-to-back SCR modules (6 SCRs). Interface to the contactor coils is

31   accomplished via a 4 pin friction lock header. This four pin connector controls the coil of

1 two bypass contactors. Each contactor accepts two wires. Interface to the Micro Monitor

2 user interface is made via a two pin spacing friction lock headers. These signals provide

3 status information to the Micro Monitor user interface regarding the static switch driver

4 board. These signals interface with the Micro Monitor user interface via an optical

5 coupler located on the Micro Monitor user interface. Interface to the system switchgear

6 board is made via a friction lock, four position header. Two wires (signal and return) on

7 the connector carry status information from the static switch driver board to the system

8 switchgear board. The remaining two wires on the connector carry the control power for

9 the pulse transformers used on the SCR drive circuitry and the FETs that drive the bypass

10 contactor coils. Though these signals are strictly used by the static switch driver board to

11 provide power to the pulse transformers and the bypass contactor FETs, they are routed

12 through a normally closed contact on the switchgear board. The contact and its

13 associated logic at the switchgear board disable the control power to the SCR drives and

14 the contactor coils when the emergency power off is initiated or when the static switch is

15 disabled through the LBS option. The static switch driver board also interfaces to the

16 power supply board via a 10 position friction lock header. Twenty-four volts DC is used

17 exclusively to power the contactor coils. The static switch driver logic disables the

18 contactors and inhibits the SCR drives if the bypass power supply voltage is not within

19 the acceptable range. The power supply board also communicates the status of the 24

20 VDC power to the static switch driver board via a digital signal. The power supply board

21 also provides control power supply for the static switch driver board, from which the +12

22 VDC and +5 VDC are derived for the static switch driver logic.

23   e) Micro Monitor User Interface

24   The Micro Monitor user interface provides the user interface for the UPS system.

25 A diagram of the Micro Monitor interface system is shown in Figure 4. Micro Monitor

26 interface 19 communicates with the user by way of keypad 27 and LCD screen 28. The

27 Micro Monitor interface may also communicate with other devices such as a personal

28 computer 29, a modem 30, or a computer network 31 by means of RS232 communication

29 ports. Micro Monitor interface board 19 also includes an RS485 connection for the

30 SITESCAN™ network system 32. The final connection to Micro Monitor interface

31 board 19 is a controller area network ("CAN") connection to control board 15. This

1 provides internal communications with the control board from the Micro-Monitor user
2 interface 19.

3 The main function of the Micro Monitor is to provide a user interface. Detailed
4 UPS parameters and alarm statuses are available to the user through a graphics LCD.
5 Another function of the Micro Monitor is to communicate these parameters to external
6 devices for local and remote monitoring. The Micro Monitor may be used in three
7 configurations: (1) single module system, (2) system control cabinet, and (3) multi-
8 module unit. All configurations use the same bare board. The Micro Monitor is designed
9 with a 16 bit AMD processor that is an 80186 derived architecture. The processor has
10 built in glue logic and built in dual asynchronous UART.

11   f) Voltage Current and Temperature Sensor Board

12 Another UPS control system component is the voltage current and temperature
13 ("VIT") sensor board 20. The purpose of the VIT board is to condition analog voltage,
14 current and temperature signals to levels suitable for analysis by the UPS control board.
15 The various VIT board connections are illustrated in Figure 7.

16 The VIT board also includes seven temperature inputs 41. These temperature
17 inputs measure three heat sink temperatures throughout the system, the inlet air
18 temperature, the battery cabinet temperature, and the exhaust air temperature. A spare
19 temperature sensor input is also provided. The VIT board processes the temperature
20 signals to levels suitable for processing by control board 15.

21 The VIT board also includes Hall effect current sensors for measuring certain DC
22 currents in the system. The DC currents measured are the rectifier output current (on
23 dual rectifier UPSs only), the battery current (the same sensor is used for measuring
24 charge and discharge current), and the inverter output current (all three phases). The VIT
25 board also measures the current through DC capacitor 42.

26 The VIT board interfaces with a control power supply that provides 24 VDC
27 power. The control power interface is made indirectly via the control board, which
28 conditions the 24 VDC to provide +/- 12VDC and 5VDC for the VIT board. VIT board
29 20 is also connected to LBS Interface board 23 for control of the optional load bus
30 synchronizing system.

The signals from the VIT board are converted to a digital format on the control board via simultaneous sampling analog to digital (A/D) converters. The simultaneous sampling A/D converters allow the three phase voltages and currents used by the control to be measured at the same moment in time. This sampling technique simplifies and improves the accuracy of the control by eliminating measurement delay between the sampled signals.

g) High Voltage Board

The VIT board also interfaces with high voltage board 21. The high voltage board attenuates system voltages to levels suitable for processing by the VIT board and the control board. The high voltage board limits its outputs to no more than 40 volts peak. Voltages measured by the high voltage board include: (1) voltage at AC input 1, (2) voltage at input harmonic filter 11, (3) voltage on bypass current path 8, (4) DC output voltage of rectifier/charger 2, (5) battery voltage 3, (6) inverter input voltage 4, (7) output LC filter voltage 12, (8) output filter fuse voltage 13, and (9) UPS output voltage.

h) Burden Board

The burden board interfaces all the current transformers ("CTs"), used to measure AC currents' to the VIT board. Each burden board input is a CT 44. Burden board inputs include the current along the first power path 9 and the current at the output 6. Both the input and output currents are three-phase currents, although the input current may be measured using only two CTs. Connection between the VIT board and the burden board is made via a twenty-wire ribbon cable. The burden board provides terminating resistors for the CTs. The resulting voltage signals are routed to the VIT board via the 20 pin ribbon cable connector. After conditioning by the VIT board, the signals are routed to the control board for processing by the DSP controllers.

i) Miscellaneous Boards

Turning again to Fig. 3, another control system component is LBS Interface board 23, which provides load bus synchronization for parallel UPS operation. The UPS control system also includes the sharing board. The sharing board is provided as an interface and allows for load sharing between multiple UPS units. Connections between the control board and the sharing board are made by both discrete wire connections and controller area network ("CAN") connections. Another UPS control system component

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1   is the system switchgear board. The system switchgear board performs various control

2   and monitoring functions for various UPS components.

3   2. Communications

4   The CAN bus is a peer to peer communications bus with message fragmentation.

5   The (11 bit) CAN identifier is divided into sections. The first bit is reserved for future

6   use. The second through fifth bits are used to identify the message class, and the final six

7   bits are used to specify the Source MAC ID.

8   Messages are put into different classes. Besides helping to determine the message

9   type, the message class determines the importance / priority of the messages. Each node

10   in a system has a unique (6 bit) MAC ID. The MAC ID is used to identify the node for

11   which a message originated or the destination of a message. The most important node or

12   nodes that perform critical functions should be assigned the lowest MAC IDs, making

13   these nodes higher in priority. By putting the source MAC ID into the CAN ID, message

14   collisions can be avoided when another node transmits a message having the same

15   message class. The message from the higher priority board will take control of the CAN

16   bus.

17   The CAN protocol makes use of part of the data block for control information.

18   The data block configuration is illustrated in the table below. Within that data block is

19   the destination MAC ID, service code, any fragmentation information (if required) and

20   any related data. The MAC ID and Service Code bytes comprise the CAN data block

21   header.

22

	Contents							
Byte	7	6	5	4	3	2	1	0
0	Frag	N/U	Destination MAC ID					
1	Rs/Rq	Service Codes						
2	Data (LB)							
3	Data (HB)							
4	Data (LB)							
5	Data (HB)							
6	Data (LB)							
7	Data (HB)							

1   Frag (Fragment) Bit: This bit is used to indicate whether this message is a piece of

2 a larger fragmented message. If the bit value is zero, the message is not fragmented,

3 meaning that the message is an entire CAN message. If the frag bit value is one, the

4 message is part of a larger fragmented message.

5   Destination MAC ID: This ID is the intended destination of the message. By

6 using the Destination MAC ID, a message transmission can be addressed to a specific

7 node on the CAN bus. In other words nodes should only receive messages with a

8 matching Destination ID. The only other message ID a node should receive is a

9 Broadcast message. Broadcast messages are those messages that are received by all nodes

10 on the CAN bus. To signify that a message is a Broadcast message and meant for global

11 consumption, the Destination ID needs to be 0x3F.

12   Rs/Rq (Response/Request) Bit: This bit indicates whether this message is a

13 response to a message or a request for information. If the bit value is zero, the message is

14 a request. If the bit value is one the message is a response.

15   Service Codes: This field indicates the message function within the message

16 Class. These codes will be defined below.

17   Data: For integer values the low byte of the integer will be transmitted first data

18 byte followed by the high byte of the integer.

19   3. Control Sequencing

20   The Comms DSP plays a key role in UPS startup operations, accepting startup

21 commands from the Micro Monitor user interface, supervising the necessary steps within

22 the UPS, and confirming to the Monitor whether the startup step completed successfully.

23 Initial startup is performed by the user, who has the option of issuing each startup

24 command individually based on prompts from the Micro Monitor, known as "manual

startup" mode. Alternately the user may select the "automatic startup" mode which self-sequences the startup steps without any further user intervention. After the initial startup, the Comms DSP may also initiate "auto restarts" after certain recoverable shutdowns. For example, if a power outage lasts long enough to completely discharge the batteries, the UPS will be shut down. But when source power is restored the UPS will automatically restart and begin powering the load and recharging the batteries again.

Control system initialization is performed by the Comms DSP as depicted in Fig 8a. When the UPS control system is powered up, the Comms DSP initializes its local internal and external memory as well as the shared global memory. It then configures and initializes ites internal peripherals and input/output ports. The Comms DSP starts polling for other active nodes on the CAN communications bus, primarily looking for the presence of the Micro Monitor user interface. If the Micro Monitor is present , the Comms DSP asks it to download the system configuration settings. If the Micro Monitor is not present or does not send the requested settings, the user may instead load the most recent configuration settings stored in the unit's nonvolatile memory; this is accomplished via a command from the diagnostic service terminal. The configuration information is then relayed to the Rectifier and Inverter DSPs whereupon they each start executing their control programs and begin operating the UPS. Starting the UPS system requires the following steps: (1) closing the static bypass switch contactors; (2) turning on the static bypass switch; (3) closing the input contactors; (4) starting the rectifier; (5) activating the input filter; (6) starting the inverter; (7) starting the battery; and (8) transferring the load to the UPS.

A flow chart illustrating the process of closing the static bypass switch contactors is illustrated in Fig. 8. To begin, the Comms DSP verifies that startup of the static bypass switch is not inhibited by an existing fault condition (for example, the static switch driver power supply has failed. If startup is inhibited, the UPS startup process is terminated. If startup is allowed, the Comms DSP then checks whether the static switch SCRs are firing. Closing the bypass contactors while the SCRs are firing could cause undesirable current transients. If the SCRs are active, contactor closure is disallowed, a failure is indicated, and the UPS startup process is terminated. If the SCRs are not firing, the Comms DSP then verifies that the bypass power source is qualified (*i.e.*, has acceptable

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voltage, frequency and phase rotation). If the bypass source is not qualified a failure is indicated and the UPS startup process is terminated. If the bypass source is qualified, the Comms DSP issues the command to close the bypass contactors. This command is sent to the static switch driver board, which then interfaces with the contactors.

After a short actuation delay, the Comms DSP checks the bypass contactor status signal returned by the system switchgear board. If the contactors did not close, a failure is indicated, a signal is sent to reopen the contactors, and the UPS startup process is terminated. If the contactors successfully closed, a short delay is initiated, allowing the Comms DSP to test for abnormal bypass operation. If an error is detected, the bypass contactors are reopened and the UPS startup process is terminated. If the qualification test passes, the startup procedure may continue.

The second step in the UPS restart sequence is starting the static bypass switch. A flow chart illustrating this process is provided in Fig. 9. To begin, the Comms DSP verifies that startup of the static bypass switch is not inhibited by an existing fault condition. If startup is inhibited, the UPS startup process is terminated. Otherwise, the Comms DSP then verifies that the bypass contactors are still closed. If the bypass contactors are open, a failure is indicated and the UPS startup process is terminated. If the bypass contactors are still closed, the Comms DSP issues a command to the Inverter DSP to begin firing the static switch SCRs. After a short delay, the Comms DSP checks the bypass status signals returned by the Inverter DSP to verify the bypass is operating properly. If a failure is indicated, the bypass SCRs are turned off, a failure is indicated, and the UPS startup sequence is terminated. If there is no bypass failure indicated, the restart sequence continues with closing the input contactor.

A flow chart illustrating the procedure for closing the input contactor is illustrated in Fig. 10. To begin, the Comms DSP verifies that startup of the UPS is not inhibited by an existing fault condition. If startup is inhibited the UPS startup process is terminated. If startup is not inhibited, the Comms DSP then verifies that the UPS input power source is qualified (*i.e.* has acceptable voltage, frequency and phase rotation.) If the input source is not qualified a failure is indicated and the UPS startup process is terminated. If the input source is qualified, the Comms DSP issues the command to close the input contactor.

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1   This command is sent to the static switch driver board, which then interfaces with the

2   contactor.

3   After a short delay, the Comms DSP checks the input contactor status signals

4   returned by the system switchgear board. If the contactor did not close, a failure is

5   indicated, a signal to reopen the input contactor is issued, and the UPS startup process is

6   terminated. If the input contactor did close, a short delay is initiated allowing the Comms

7   DSP to test for abnormal system operation. If a failure is detected, the input contactor is

8   reopened and the UPS startup process is terminated. If the post-actuation qualification

9   test passes, the startup procedure may continue with rectifier startup.

10   A flow chart illustrating the rectifier startup process is shown in Fig. 11. To begin,

11   the Comms DSP verifies that startup of the UPS is not inhibited by an existing fault

12   condition. If startup is inhibited the UPS startup process is terminated. Otherwise the

13   Comms DSP then verifies that the input contactor is still closed. If the input contactor is

14   open, a failure is indicated and the UPS startup process is terminated. If the input

15   contactor is still closed, the Comms DSP sends a command to the Rectifier DSP to start

16   the rectifier. The Rectifier DSP will then begin to fire the rectifier devices and "walk in"

17   the rectifier.

18   Rectifier walk-in and firing angle control are explained in detail later in this

19   document. The Comms DSP maintains a timeout counter while the rectifier walk-in

20   occurs. The Comms DSP monitors the status of the rectifier status flags set by the

21   Rectifier DSP, indicating whether walk-in is done and the DC bus voltage is within

22   limits. If walk-in has not completed before the timeout period ends, the Comms DSP

23   disables the rectifier and the UPS startup process is terminated. If walk-in completes

24   within the timeout, a short delay is initiated allowing the Comms DSP to test for

25   abnormal rectifier operation. If a rectifier failure exists, the Comms DSP disables the

26   rectifier and the UPS startup process is terminated. If there is no rectifier failure the

27   startup process may continue.

28   A flow chart of steps required to start the input filter is illustrated in Fig. 12. As

29   soon as the rectifier has successfully started, the Comms DSP sends a command to the

30   switchgear board to close the input filter contactor. After a short actuation delay, the

31   Comms DSP checks the input filter contactor status returned by the system switchgear

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1   board. If the contactor did not close, a failure is indicated and a signal to reopen the input

2   filter contactor is sent. If the contactor did close, a short delay is initiated allowing the

3   Comms DSP to test for abnormal filter operation (for example, testing for a blown filter

4   fuse.) If a failure is detected, the input filter contactor is reopened. Regardless of

5   whether the input filter activation completed successfully or not, the UPS startup process

6   is allowed to continue.

7   A flow chart illustrating the inverter startup process is shown in Fig. 15. First the

8   Comms DSP verifies that startup of the UPS is not inhibited by an existing fault

9   condition. If startup is inhibited the UPS startup process is terminated. Otherwise the

10 Comms DSP then verifies that the DC bus voltage is qualified, based on a status flag

11 from the Rectifier DSP. If the DC bus is not qualified, a startup failure is indicated and

12 the UPS startup process is terminated. If the DC bus is qualified, the Comms DSP issues

13 an Inverter Enable command to the Inverter DSP. The Inverter DSP begins firing the

14 inverter output devices. After a short delay, the Comms DSP checks the inverter status

15 signals returned by the Inverter DSP to verify the inverter is operating properly. If a

16 failure is indicated, the Comms DSP will disable the Inverter, indicate a startup failure,

17 and terminate the UPS startup sequence. If no errors were encountered, then the inverter

18 startup is complete and UPS startup continues with the battery system.

19   The sixth step in starting the UPS is to bring the battery online. A flow chart for

20 the battery startup process is illustrated in Fig. 14. Again, the Comms DSP verifies that

21 startup of the UPS is not inhibited by an existing fault condition. If startup is inhibited

22 the UPS startup process is terminated. The Comms DSP then verifies that the rectifier is

23 running. If the rectifier is not running, a failure is indicated and the UPS startup sequence

24 is terminated. If the rectifier is still running, the Comms DSP verifies that the DC bus

25 voltage is equal to the DC bus nominal setpoint, which indicates that the Rectifier DSP is

26 operating correctly. If it is not, a failure is indicated and the UPS startup process is

27 terminated. If the rectifier controller is functioning correctly, then the Comms DSP

28 checks that the battery voltage is greater than the battery End-of-Discharge voltage,

29 which verifies that the battery is present. The principle of this test is that the open circuit

30 battery voltage is always greater than the loaded battery voltage at full discharge. If the

battery is not present, the Comms DSP indicates a failure and the UPS startup process is terminated. If the battery is present then the battery startup process continues.

The Comms DSP then issues a "start battery" command to the Rectifier DSP. The Rectifier DSP reduces the DC bus voltage to match the battery voltage, which prevents a large inrush current when the battery circuit breaker is closed. Large inrush currents cause negative electrochemical reactions in the battery that shorten battery life. Such currents are advantageously avoided by the UPS of the present invention. The Rectifier DSP then sets the battery current limit to zero in preparation for battery "walk-in". The details of rectifier control for battery walk-in are described below. When this process is finished, the Comms DSP then enables the undervoltage coil in the battery circuit breaker.

The Comms DSP then checks whether the battery circuit breaker is manually operated or motorized. If the battery circuit breaker is manually operated, the user is prompted to close the circuit breaker, thereby connecting the battery to the DC bus. The Comms DSP maintains a timeout counter while the breaker closure occurs. The Comms DSP constantly monitors the battery circuit breaker status from the switchgear board to determine when the user closes the breaker. If the battery breaker does not close before the timeout period ends, the Comms DSP will trip the battery breaker, signal an error, and discontinue startup. The Rectifier DSP returns the battery voltage and current setpoints to their nominal values. If the battery breaker is closed before the timeout expires, the battery startup process continues.

If the battery circuit breaker is motor operated, the Comms DSP starts the battery circuit breaker motor operator. The Comms DSP then waits for the signal from the switchgear board that the battery circuit breaker has closed. If the battery circuit breaker does not close before the timeout period ends, the Comms DSP indicates a failure, disables the undervoltage coil on the battery circuit breaker (i.e. trips the battery breaker) and terminates the UPS startup sequence. The Rectifier DSP returns the battery voltage and current setpoints to their nominal values. If the battery circuit breaker closes within the timeout period, the battery circuit breaker motor operator is stopped to prevent overrun. If the breaker successfully closes, the battery startup sequence continues.

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The next step in the battery startup sequence is battery walk-in. The Rectifier DSP will reset the DC bus voltage setpoint to its nominal level, but because the battery current limit is still at zero, the DC bus voltage will remain at the battery float voltage. The battery current limit setpoint is then gradually increased from zero to nominal over a span of several seconds, controlling the rate of change of the battery charging current. The resultant smooth charging current prolongs the service life of the battery. The exact duration of the battery walk-in is not critical, but longer times improve battery life. As the current is ramped up, the DC bus voltage gradually returns to its nominal value.

At the end of the battery current limit ramp, a short delay is initiated. This delay allows the Comms DSP to check for abnormal battery operation. If an error is discovered, the battery breaker is tripped, the setpoints are returned to their nominal values, and the UPS startup sequence is terminated. If there are no errors the UPS is ready for the load to be transferred from the bypass to the UPS. The transfer process is detailed in the Inverter DSP operation later in this document. If the transfer to UPS is successful, the UPS startup procedure is complete. If it is unsuccessful, an error is indicated and the UPS startup sequence is terminated.

If the UPS reports that any critical step in the startup sequence fails, the Micro Monitor issues a shutdown command to the Comms DSP, which then sequentially turns off the UPS devices in the reverse order of startup.

II. OVERALL CONTROL

A. Global Memory Mapping/Arbitration

The function of global memory is to allow several processors to have secure read and write access to a single memory device. This function allows the processors to communicate critical data on a processor instruction cycle basis. The global memory function can generally be created in two different configurations. The first configuration uses address buffers with tri-state outputs, bi-directional data transceivers with tri-state inputs/outputs, a complex programmable logic device (CPLD) and a memory device. The second configuration uses a programmable crosspoint switch (which takes the place of the buffers and transceivers), a CPLD and a memory device.

In both configurations a CPLD is programmed to provide global memory arbitration. This arbitration is priority driven with the first processor in the scheme

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1   having the highest priority and the last processor having the lowest priority to access the

2   global memory. The priority scheme is also non-preemptive in that once a processor is

3   granted access to the global memory no other processor can gain access until the

4   processor that is currently accessing the global memory is finished. Once the global

5   memory is available to be accessed the processor with the highest access priority is

6   granted access first. This scheme provides secure access to a memory location and thus

7   prevents the data from being changed by more than one processor at a time.

8   In both configurations the memory device can be of any memory size, data width

9   and speed grade. Also, the address buffers and data transceivers or the crosspoint switch

10   serves as a means to share the memory device's address and data busses among several

11   different processors without the possibility of having bus contention. The arbitration

12   circuit is illustrated in Fig. 35.

13   The memory arbitrator has two input control lines from each DSP. One control

14   line is used to indicate that an external bus cycle is commencing and is used for timing

15   synchronization. The other control line is asserted to request access to the external global

16   memory device. In this implementation, the two control signals are defined as strobe and

17   bus request. When these signals are active from the DSPs with a higher priority than the

18   lowest priority DSP, a lock signal is generated. The DSP with the highest lock priority is

19   granted access to the global memory by the arbitration logic generating the necessary

20   global memory chip select, DSP ready signal, crosspoint switch multiplexer and enable

21   signals and the memory read or write signals. In the event that the lowest priority DSP

22   has access to the global memory, the chip select signal serves as the lock signal to

23   prevent higher priority DSPs from accessing the global memory.

24   B. Message Fragmentation

25   The fragmentation method implemented in the UPS of the present invention is

26   similar to DeviceNet's Fragmentation for Explicit messages, but it differs being that this

27   protocol is a Peer to Peer implementation as opposed to DeviceNet's connection based

28   system (ref. 1). What makes fragmented messaging possible in this peer to peer

29   implementation is the presence of a busy acknowledgement and handling of conditions

30   when a node's fragmentation service is busy processing another fragmented message.

1 Message Fragmentation allows for the transmission of messages that cannot fit

2 into the eight byte data block of the CAN message. Message Fragmentation segments a

3 larger message into smaller fragments to be sent over the CAN bus. When the fragments

4 are received they are reassembled into the larger message.

5 The fragmented Data block is similar to the normal data block with the exception

6 that another byte is allocated for message fragmentation control as shown in the table

7 below.

Byte	Contents							
	7	6	5	4	3	2	1	0
0	Frag	N/U	Destination MAC ID					
1	Rs/Rq	Service Codes						
2	Frag. Type		Fragment Count					
3	Data							
4	Data							
5	Data							
6	Data							
7	Data							

8 Frag. (Fragment) Type: The fragment type indicates whether this message is the

9 first, one of the middle or the last fragment transmissions of the larger message.

10 A fragment type value of zero indicates that the fragment is the first fragment of

11 the message. The fragment count is zero for the first fragment or Ox3F if the fragment is

12 the first and last fragment. A fragment type value of 1 indicates that the fragment is one

13 of the middle fragments. A fragment type value of 2 indicates that the fragment is the

14 last fragment. A fragment type value of 3 is used to acknowledge the reception of a

15 fragmented message.

16 Fragment Count: This indicates which fragment block this message is out of the

17 entire message. The receiver can monitor this field to determine if a fragment has been

18 lost or skipped. The fragment count is incremented for each fragment in a series. Counts

19 higher than 63 will cause the counter to roll over to 0 and continue to count. This does

20 not mean fragmented messages have to be limited to 64 fragmented CAN messages.

21 When a message fragment is acknowledged another byte is used to indicate the

22 success of the transmission.

CAN Message Format For Fragmented Messages:

Byte	Contents							
	7	6	5	4	3	2	1	0
0	Frag	N/U	Destination MAC ID					

1   Acknowledge Status: The Fragment Acknowledge Status indicates the reception

2   success of an individual fragment message. A fragment acknowledge status value of O is

3   used to indicate a pass or successful reception. A value of zero indicates a fail (too much

4   data), and a value of 2 indicates the receiver is busy.

5   The transmission of a Fragmented message is a hand shaking process. As each

6   fragment is transmitted, it is acknowledged by a return message from the receiving node

7   as to whether it was processed successfully or not (Pass/Fail/Busy). To start the process

8   the transmitting node sends the first fragment over the CAN bus. If the receiving node is

9   able to receive the message (it has a fragmentation service available) it will acknowledge

10   the transmission with a Pass condition. This process will continue until the entire

11   Fragmented Message is received.

12   If the receiving node is busy processing another node "A" Fragmented Message,

13   the receiving node cannot support the reception of the first fragment from node "B". As a

14   result the receiving node will acknowledge node "B" with a Busy. After a predetermined

15   delay time, the sending node will try again to send the First Fragment and again wait for

16   an acknowledge.

17   Similar to the transmit timeout waiting for a transmit acknowledge, the receiving

18   node will run a timeout on the reception of the next fragment. Once the receiving node

19   has received a valid fragment and acknowledged it, the receiving node will start a timer.

20   If the timer should expire before the reception of the next fragment, the Receive

21   Fragment service will be set to the initial state (de-allocating the service), and the

22   fragments received to this point will be abandoned.

23   Transmit Fragment Service Operations:

24   Check to see if the Transmit Fragmented Message Service is available. If the

25   service is Busy it will be indicated as such to the calling routine, or the message will be

1 stored in a queue for later processing. The Transmit Fragmented Message Service is Busy

2 because it is being used by another task for Fragmented Message transmissions.

3 If available, the service will be allocated so that no other task may interrupt this

4 message fragmentation. The service will then build the first message fragment.

5 The message fragment will then be transmitted, and "a wait for acknowledge

6 timer" is started. The wait time is application specific and may even be message specific.

7 For an acknowledgement to be received it must be from the intended destination (MAC

8 ID) and have the same message class and service code.

9 If an acknowledge is not received within the wait time, the Message Fragment

10 will be transmitted again. If for a second time a Message Fragment is not received within

11 the timeout period, then the calling application is informed that an error has been detected

12 and that the Fragmented messaging cannot take place at this time.

13 If an acknowledgement is received as a Busy, a delay will be imposed on transmit

14 fragment operations then the service will retransmit the Message Fragment and wait for

15 an acknowledgement again. This will continue for a set number of attempts after which

16 the Transmit Fragmentation Service de-allocated and made available for other

17 transmissions. The delay should be a time small enough to continue message throughput

18 but not be an annoyance to the target node. The Number of attempts times the delay time

19 should be greater than the estimated throughput of the largest fragmented message in the

20 system.

21 If an acknowledgment is received, the Transmit Fragment Service will determine

22 whether or not the Fragment count in the acknowledge message is equal to that of the last

23 Fragment Message transmitted. If they are equal, the Fragment was successfully

24 delivered, and the next Fragment (if any) can be delivered. If the count is not the same,

25 the Transmit Fragment Service will continue to wait for an acknowledge with the proper

26 Fragment count.

27 Receive Fragment Service Operations:

28 If the Receive Fragmentation Service is not currently busy receiving another

29 message, the Receive Fragment Service will check to see if a received message is the first

30 Fragment of a Fragmented message. Once the first fragment has been received, the

1   Receive Fragment Service stores the message source MAC ID, Class and service code.

2   This data is used to screen out other fragmented messages that may be on the bus.

3   If the Receive Fragment Service is busy processing another fragmented message

4   or just not available, an acknowledge will be sent with a Busy signal to the sender.

5   If the fragment service is available, then the fragment Service looks to see if the

6   fragment type is the First Fragment and that the Fragment count is zero. If correct, the

7   message is stored and an acknowledge, indicating success, is returned.

8   If the Fragment count is one greater than the previous received count and the

9   fragment type does not indicate that this is the first fragment, then the fragment is

10   received and is appended to the previously received fragment. With the additional

11   fragment received, an acknowledge with a Pass signal is returned. The fragment count

12   from this fragment is stored.

13   If the fragment count is equal to the previous received fragment, the same

14   acknowledged is issued in response. No data is stored. This is due to the CAN EOF error

15   condition that can result in a message being duplicated.

16   If the Fragment count is neither one greater than or equal to the previously stored

17   fragment, then the no data is stored and no acknowledgment is issued. The Receive

18   fragment Service is reset to the Initial State.

19   If after the successful reception of a message fragment, the next message

20   fragment is not received within a specific period, the Receive Fragmentation Service will

21   be reset to the Initial State.

22   When the final fragment is received and the acknowledgment is transmitted, the

23   Receive Fragment Service resets to the initial state, making it available for other

24   fragmented messages.

25   Initial state is the condition in which the Receive Fragmentation Service is idle

26   and ready to start receiving a fragmented message. The Service has not been allocated

27   and the Fragment count is zero.

28   C. Dual Discharge Circuits

29   The UPS of the present invention also provides a mechanism whereby the battery

30   current is sensed using a single Hall effect current sensor while producing separate

31   current signals for the discharge current and charge current. In a typical UPS, the battery

1   discharge current is significantly larger than the battery charging current. Historically,

2   the differing magnitudes between the discharge current and the charging current have

3   required multiple current sensors. Specifically, the larger discharge current necessitates a

4   larger dynamic range on the sensor signal, while the smaller charging current requires a

5   finer resolution for accurate charging control. The present invention overcomes this

6   limitation of the prior art by providing a single current sensor with two amplifier circuits,

7   one providing the dynamic range required for discharge current measurement and the

8   other providing the sensitivity required for charging current measurement.

9   The battery current measurement circuit is illustrated in Fig. 25. The voltage

10   signal from the Hall effect current sensor, which represents the battery current, is applied

11   to the circuit at input 2301. The circuit includes two amplifier circuits, a discharge

12   amplifier circuit 2304, and charging amplifier circuit 2305. As noted above, the

13   discharge current is significantly larger than the charging current, and thus it is required

14   that the signal supplied to the controller DSPs have a broader dynamic range. Therefore,

15   the discharge amplifier has a lower overall gain. Conversely, because the charging

16   current is significantly less than the discharge current, it is necessary to have a higher

17   degree of resolution for the signal supplied to the controller DSPs. In the illustrated

18   circuit, the discharge amplifier 2304 has an overall gain of 1.2439, while the charging

19   current amplifier 2305 has a gain of 12.439. Although particular topologies and gains

20   have been disclosed for the amplifier circuits illustrated in Fig. 25, other amplifier

21   topologies having other circuit parameters, including other gains, may be used as well.

22   III. INPUT CONTROL

23   Control board 15 includes a second processor, the Rectifier DSP 25, also known

24   as the Input DSP. The Rectifier DSP controls rectifier/charger 2. Control tasks

25   implemented by the Rectifier DSP include: (1) implementation of the zero cross detector

26   or phase locked loop ("PLL") for rectifier timing and synchronization, (2) rectifier firing

27   angle control, (3) load step detection, (4) adaptive switching control to compensate for

28   the phase rotation of the supplied AC voltage, and (5) input qualification. The Rectifier

29   DSP also performs control functions related to source sharing where AC input 1 is

30   connected to more than one source of AC Power. Finally the Rectifier DSP controls

31   various analog setup and digital inputs to the control board. These control functions

1   include: multiplexer control, reading the analog to digital converters, applying calibration

2   constants to the analog inputs, saving the instantaneous analog input values, and

3   populating the analog RMS value arrays, reading the digital input ports, updating the

4   status variables in memory, and writing to the digital output ports.

5   A. Rectifier Timing and Synchronization

6   The Rectifier DSP generates and outputs the firing signals for the rectifier. The

7   Rectifier DSP outputs the firing signals to the SCR driver board 16, which fires the SCRs

8   in the desired sequence. The Rectifier Driver, item 16 in Fig. 3, receives the individual

9   SCR firing signals and converts them to a "picket fence" gate drive by combining an on

10   board free running oscillator signal with the SCR firing signal. The oscillator is a thirty

11   percent duty, 15 kilohertz rectangular pulse. A simple logical AND of these two signals

12   would result in varying delay in the gate signal of up to two thirds of a cycle of the 15

13   kilohertz oscillator. This varying delay causes unacceptable performance and can be

14   eliminated by adding a one-shot timer triggered by the rising edge of the SCR firing

15   signal which is then logically ORed with the free running oscillator. The rectifier drive

16   pulse generation circuitry is illustrated in Fig. 38.

17   The phase angle of the supplied utility voltage is required by the UPS system to

18   accomplish synchronization of the rectifier SCR firing. A digitally-implemented,

19   software zero cross detector or PLL is used to extract the phase angle from the incoming

20   utility voltage. Because of the critical control tasks that require accurate phase angle

21   information, it is desirable that the output of the zero cross detector or PLL be insensitive

22   to distortions on the input AC line.

23   1. Zero-Cross Detection

24   The zero cross detector provides the phase synchronization information for the

25   firing angle controller of the silicon controlled rectifiers ("SCRs") that make up the

26   rectifier/charger. Each phase is independently controlled relative to its own zero cross

27   detection. The zero cross detector is online at all times, including times that the input line

28   is unqualified and the rectifier is offline. Input line qualification is performed by the

29   control system and includes measurements of the voltage, frequency and phase rotation

30   of the incoming line and verifying that they are within the specified operating ranges. The

31   zero cross detector will operate properly with either clockwise or counter-clockwise

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1 rotation of the incoming three-phase line, which allows the rectifier to operate regardless

2 of the connected phase rotation.

3   In the case of the zero cross detector, each phase voltage is filtered via a low pass

4 hardware filter that provides a phase shift of 60 degrees. Since each phase of the rectifier

5 is controlled independently relative to its own zero cross detection, it is desirable that

6 each of the filters have identical phase shift values to prevent unbalanced currents

7 flowing from the input source. To accomplish this, any error in the measurements as a

8 result of filter circuit component tolerances is automatically accounted for by the

9 controller. This is done at system startup; the controller detects the zero cross of both the

10 input and output signals of each filter using this information to derive the actual phase

11 shift of each filter. Subsequently, the controller makes adjustments to each filter zero

12 cross detection such that the effective phase shifts of each filter are identical.

13   2. Digital PLL

14   In the case of the PLL, prior art PLLs suffer various performance disadvantages

15 caused by input distortion. For example, notching in the input waveform causes

16 harmonic distortion in the PLL output. Similarly, loss of input voltage on one or more

17 phases results in a loss of PLL gain and a corresponding reduction or loss of output,

18 causing the PLL to stop tracking the input. Finally, another shortcoming of prior art

19 PPLs is that input phase deviation would increase the PLL error signal and distort the

20 sinusoidal output angle signal.

21   A control diagram of the digitally implemented PLL used in the present invention

22 is illustrated in Fig. 16. The line to line input voltages (V_{ab}, V_{bc}, and V_{ca}) are sampled,

23 and the sampled voltages are passed through a finite impulse response ("FIR") filter. The

24 FIR filter produces the filtered voltages V_{ab_f}, V_{bc_f}, and V_{ca_f}. The FIR filter eliminates

25 relatively low frequency distortion ("harmonics") from the sampled voltages. Harmonic

26 frequencies up to one-half the sampling frequency are trapped by the filter. The FIR

27 filter is digitally implemented by the Rectifier DSP. Implementation of such filters is

28 well known in the prior art.

29   The filtered voltages are then transformed into the DQ rotating reference frame.

30 The DQ rotating reference frame is synchronized to the utility frequency.

31 Synchronization is maintained by PLL output angle feedback. Rectifier PLL control is

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performed in the DQ rotating reference frame to minimize the processor power required for rectifier control. The transformation into the DQ rotating reference frame is well known in the prior art and is mathematically expressed by the following equations:

$$V_{QS} = V_{ab}$$

$$V_{DS} = \frac{(V_{ca} - V_{bc})}{\sqrt{3}}$$

$$V_{QE} = V_{QS} \cdot \cos(\theta) - V_{DS} \cdot \sin(\theta)$$

$$V_{DE} = V_{QS} \cdot \sin(\theta) - V_{DS} \cdot \cos(\theta)$$

where V_{ab}, V_{bc}, and V_{ca} are the three phase line-to-line voltages, V_{QS} and V_{DS} are the stationary DQ reference frame voltages, V_{QE} and V_{DE} are the rotating DQ reference frame voltages, and θ is the output angle of the phase locked loop.

After the DQ transformation, the Q-axis voltage is selected as the control variable. By manipulation of the equations above, it can be shown that the angle error between the reference voltage and the output voltage determines the magnitude of the D-axis and the Q-axis voltages. If the angle error is set to zero, the D-axis voltage is equal to the magnitude of the line voltage and the output angle may be locked to the input by regulating the Q-axis voltage to zero.

The error between the Q-axis voltage and the zero setpoint is passed through a proportional-integral ("PI") controller to produce the rotational frequency of the DQ reference frame. By generating this frequency it is possible to lock to the utility frequency at any arbitrary phase. By integrating the derived utility frequency, the phase angle of the utility voltage may be obtained. However, the FIR filter applied to the input voltage causes a delay that skews this phase angle. Thus the phase angle must be corrected to compensate for the delay introduced by the FIR input voltage filter. Using the known properties of the filter, which are parameters selected by the filter designer, it is possible to determine the filter delay and adjust the derived phase angle by a corresponding amount. The filter delay is given by:

$$D_f = \frac{N-1}{2}$$

where D_f is the filter delay in samples and N is the filter length. Given the filter delay, the corresponding phase delay is given by:

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$$D_\theta = \frac{F_{LPF} \cdot 360^\circ \cdot D_f}{F_{sample}}$$

where D_θ is the phase delay, F_{LPF} is the frequency of the incoming line after low pass filtering, D_f is the filter delay in samples, and F_{sample} is the sampling frequency. Thus the corrected filter angle is:

$$\theta = \theta_f + D_\theta$$

where θ is the corrected angle of the source voltages, θf is the uncorrected angle of the filtered source voltages, and $D\theta$ is the phase angle delay.

The goal of the software PLL algorithm is to provide angle and frequency information about the input source to the rectifier firing angle controller. Unlike the inverter PLL discussed below, the rectifier PLL is not restricted to a low slew rate. In fact, a high rectifier PLL slew rate in that it allows quick response to load changes without DC bus voltage and battery current disruptions. The basic control algorithm operates by determining the difference between the input phase angle and the PLL output. If this difference is positive then the PLL output frequency is increased to catch up to the input phase angle. If the difference is negative, the PLL output frequency is decreased so that the input phase angle will catch up with the PLL output phase angle.

B. Rectifier Firing Angle Control

Regardless of how the phase angle information is derived, rectifier firing angle control is necessary to supply the proper amount of power to the DC bus 10. A diagram of the rectifier control system is provided in Fig. 17. The rectifier controller is a classical PI feedback control loop that is tuned to regulate the DC bus voltage to some nominal voltage setpoint. The difference between the actual bus voltage and the setpoint is the error signal into the PI control. The output of the PI control loop represents the desired rectifier firing angle.

Normally, if both input current and battery charge current are below their respective limits, then the control operates as described in the preceding paragraph. If the input current or battery charge current are at the respective limit the controller will switch its mode of operation temporarily until the out of tolerance current is back within the corresponding limit. The rectifier control mode switching scheme implemented by the UPS of the present invention reduces transients on the DC bus.

1   If the rectifier load increases such that the input current reaches the current limit
2 setpoint, the rectifier controller switches to control SCR firing based on the input current.
3 The input current is regulated to remain at the current limit setpoint, and the difference
4 between the current limit and actual input current will be the error signal to the PI
5 control. To prevent controller output discontinuity when switching between the DC bus
6 voltage control mode and the input current control mode, the PI control integrator
7 element is preset to a value equal to the total PI control output at the instant before
8 switching. The PI controller gains are then set to values tuned to control and maintain the
9 input current at the current limit setpoint. While the rectifier is in current limit control,
10 the DC bus voltage falls below the prior DC bus voltage setpoint used as the control
11 parameter before the switch to current control mode. This DC bus voltage decrease is
12 unavoidable because the required load power exceeds the available input power.

13   The rectifier controller remains in current limit control mode until the load power
14 decreases so that the required rectifier input current is below the current limit setpoint.
15 As the load decreases, the DC bus voltage returns to the voltage setpoint used as the
16 control parameter before the transfer to current limit control mode. The controller then
17 switches back to the normal voltage control mode. The voltage error signal is the input to
18 PI loop and the controller gains are reset to the original values used for voltage control.
19 To again provide a seamless control mode transfer, the integrator is preloaded to the
20 control loop output value immediately before the control mode transition.

21   If the battery charging current exceeds the limit setpoint, the rectifier controller
22 continues to operate in voltage control mode; however, the DC bus voltage setpoint is
23 lowered from its nominal value to a value that will maintain the battery charging current
24 at the limit setpoint. The controller continues to operate in this mode, maintaining charge
25 current at the limit. As the battery charges, the battery voltage increases. The DC bus
26 voltage setpoint increases correspondingly, which maintains the battery charging current
27 at the limit setpoint. As the battery charge increases further, the battery voltage continues
28 to increase until it reaches a point that the nominal DC bus voltage setpoint does not
29 cause the charging current to exceed the charging current limit setpoint. At this point, the
30 rectifier controller has returned to its normal voltage control mode using the nominal
31 voltage setpoint determined by the control system for the present operating conditions.

C. Load Step Detection

The Rectifier DSP must control the rectifier such that sufficient power for the critical load is delivered to the DC bus. It is therefore critical that the rectifier controller, i.e., the Rectifier DSP, detect a change in the load on the UPS and adjust the rectifier accordingly. If the load suddenly increases, the firing angle must be increased to supply more power to the DC bus. Conversely, if the UPS load decreases, the rectifier firing angle must be decreased to reduce the power supplied to the DC bus. Without rapid firing angle control, if the load is drastically increased the extra power required must be supplied by the battery. Conversely, if the load decreases drastically, the excess energy will be absorbed by the battery. In either case, a large change in the battery current occurs, which is detrimental to battery life.

Prior art rectifier controllers typically include a derivative term added to the PI controller (making it a PID controller) for controlling the rectifier under transient load conditions. This term is added to prevent excessive DC bus voltage excursions when the UPS load changes, i.e., to prevent overvoltage on a major load decrease or under voltage on a major load increase. This classical prior art solution creates problems in controlling the DC bus voltage in the presence of steady state unbalanced or crest load conditions. The derivative term of the controller responds to the variations caused by the unbalance or crest load and causes constant rectifier firing angle changes. This constant firing angle "hunting" is undesirable because it causes unnecessary input current variations. A better solution to this problem, which is implemented by the UPS of the present invention, is to remove the derivative term in the controller and add some non-linear element to respond to DC bus voltage transients caused by significant load changes. Another possible solution is implementation of a fuzzy logic algorithm.

The solution implemented for the rectifier controller of the present invention is as follows: if the DC bus voltage deviates from the setpoint value by more than some predefined limit, and the DC bus voltage rate of change exceeds some predefined limit, then the rectifier firing angle is modified to compensate for the load change. Rectifier firing angle compensation is accomplished by adding some predefined value to the integrator term. The value is determined by the DC bus voltage value and rate of change. This control technique prevents excessive DC bus voltage excursions caused by UPS load

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1   changes. This technique also prevents the rectifier from responding to small DC bus

2   voltage variations caused by an unbalanced or crest load.

3   The Rectifier DSP implements rectifier walk-in control on startup. The input

4   walk-in rate is adjustable. At startup, the Rectifier DSP limits the DC bus voltage rate of

5   increase by ramping the DC bus setpoint from zero to the nominal DC bus setpoint over a

6   10 second period. The DC bus voltage rate of increase to approximately 54 volts per

7   second for a nominal setpoint of 540 volts. During voltage walk-in, the Rectifier DSP

8   also controls the input current rate of increase and the battery charging current rate of

9   increase. The rate at which these limits rise toward their nominal values may be

10   configured by the user.

11   D. Phase Compensation

12   The Rectifier DSP also modifies the rectifier switching sequence to compensate

13   for the phase rotation of the input voltage. A three phase electrical system has two

14   possible phase rotations or phase sequences, clockwise and counter clockwise. Prior art

15   UPS systems implemented a fixed SCR firing sequence, which required that the

16   incoming AC line be connected in the correct sequence. If any two of the incoming leads

17   were reversed, the system would not operate properly because of the incorrect phase

18   rotation. In the present invention, the Rectifier DSP can detect the input phase rotation

19   and alter the SCR firing sequence to adapt to the connected phase rotation.

20   When either the battery charging current or the input current begins to rise above

21   zero, the corresponding current limit setpoint begins to ramp from zero to the nominal

22   value for that current limit. During the walk-in, if the input current and battery charge

23   current are below their respective limits, the DC bus setpoint is increased toward the

24   nominal setpoint. However, if either input current or battery charging current is above its

25   corresponding limit, the DC bus voltage setpoint is held at the present DC bus voltage.

26   Holding the DC bus voltage setpoint prevents the Rectifier DSP from advancing the

27   rectifier firing angle, thereby limiting the current to the desired value. Once both currents

28   fall below their respective limits, the DC bus setpoint again begins to increase.

1   E. Battery Charging

2   1. Battery Charging Modes

3   The Rectifier DSP also controls battery charging process. Control of the battery

4   charging process includes implementing "battery saver" and "turbo" charging modes

5   discussed above. The different charging speeds are implemented by setting a battery

6   charging current limit setpoint that corresponds to either the slower or faster charging

7   rate. These limits are then used for charging control as discussed throughout the

8   description of the Rectifier DSP.

9   2. Temperature Compensation

10   The Rectifier DSP is also programmed to implement temperature compensated

11   battery charging. The compensation circuitry includes a thermistor input into the

12   Rectifier DSP. The thermistor measures the temperature inside the battery cabinet. The

13   Rectifier DSP processes this temperature and adjusts the battery current limit setpoint

14   accordingly. The battery current limit setpoint affects the DC bus voltage as described in

15   the battery walk-in description.

16   F. Input Qualification

17   Various other rectifier control functions are implemented by the Rectifier DSP.

18   For example, the Rectifier DSP must verify the input line qualification. Input line

19   qualification includes verifying that the supplied voltage, frequency and phase rotation

20   are acceptable to operate the UPS in its present configuration. To determine whether the

21   incoming line is within an acceptable tolerance, the Rectifier DSP monitors voltage,

22   frequency and phase rotation. The fact that the UPS of the present invention is designed

23   to be applied on a three phase power system means that the UPS can determine whether

24   these parameters are within an acceptable range by monitoring only one parameter one

25   each phase. This also enables the DSP to detect a single phase fault on any of the three

26   phases. For example, by monitoring the voltage on phase A, the frequency of phase B,

27   and the phase sequence between phase C and either phase A or B the Rectifier DSP will

28   detect any voltage, frequency, or rotation failure due to interactions among the phases.

29   This detection method also permits the detection of any single phase failure because the

30   corresponding three phase parameter will also be missing.

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1   Even when the input line is not qualified, the Rectifier DSP is programmed to

2 draw as much power as the line is capable of delivering up to the rectifier current limit.

3 The UPS system will make up any power deficit between the power required by the

4 critical load and the power available from the line by drawing power from the battery.

5 This minimizes the amount of battery power drain, thereby prolonging battery life.

6 IV. OUTPUT CONTROL

7   Control board 15 includes a third processor, the Inverter DSP 26, which is also

8 known as the Output DSP. The Inverter DSP controls inverter 4 and bypass static switch

9 5. Inverter DSP control functions may be categorized in one of the following six

10 categories: (1) inverter PWM control, (2) advanced output control, (3) bypass static

11 switch control, (4) transfer control, (5) parallel/multiple unit control, and (6) processor

12 input and output control.

13   A. Inverter PWM Control

14   The first group of inverter control functions relates to PWM control, such as

15 generating the reference sine wave. The Inverter DSP causes the inverter to track the

16 bypass input voltage if the bypass is qualified. Otherwise, the inverter runs

17 independently. Using the reference sine wave the Inverter DSP also generates the PWM

18 signals and the inverter IGBT firing signals.

19   Space vector PWM is a technique for determining the switching sequence of the

20 transistors making up the inverter. Space vector PWM results in less harmonic distortion

21 in the inverter output and also provides more efficient use of the DC supply voltage than

22 other PWM techniques. For the description following, it is useful to map all of the

23 voltages into the DQ reference frame, which is performed by a standard transformation

24 well known to those of skill in the art. The transformation is implemented using the

25 following equation:

$$
\begin{bmatrix} V_{Ds} \\ V_{Qs} \\ V_{0s} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{\sqrt{3}}{3} & \dfrac{\sqrt{3}}{3} \\ \dfrac{2}{3} & -\dfrac{1}{3} & -\dfrac{1}{3} \\ \dfrac{1}{3} & \dfrac{1}{3} & \dfrac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix}
$$

26

where V_{Ds}, V_{Qs} and V_{0s} are the DQ axis voltages (note that $V_{0s}=0$ if the voltages are balanced) and V_A, V_B, and V_C are the three phase voltages. This mapping results in the eight possible output vectors illustrated in Fig. 21. (Two of the vectors are actually zero vectors in DQ coordinate space, and thus only the six non-zero vectors are shown.)

The desired output voltage required by the control system may also be mapped into DQ space, resulting in a DQ command voltage vector. The objective of the space vector PWM technique is to use the eight possible switching states of the inverter switching devices to approximate the command voltage vector. This is accomplished by time averaging of the available output voltage vectors. An example is illustrated in Fig. 22. Assuming a command voltage vector $|V_{cmd}|\angle\alpha_{cmd}$, which lies between the output vectors V_3 and V_2, the output voltage to match the command vector may be approximated by time applying vector V_3 for a time T_1, vector V_2 for time T_2 and either vector V_7 or vector V_8 for time T_0. The times for application of the various voltage vectors are given by the following equations:

$$T_1 = T_{PWM} \cdot \frac{|Vcmd|}{V_{DC}} \cdot \left[\cos\left((k-1)\cdot\frac{\pi}{3} - \frac{\pi}{6} \right) \cdot \sin(\alpha) - \sin\left((k-1)\cdot\frac{\pi}{3} - \frac{\pi}{6} \right) \cdot \cos(\alpha) \right]$$

$$T_2 = T_{PWM} \cdot \frac{|Vcmd|}{V_{DC}} \cdot \left[\sin\left(k\cdot\frac{\pi}{3} - \frac{\pi}{6} \right) \cdot \cos(\alpha) - \cos\left(k\cdot\frac{\pi}{3} - \frac{\pi}{6} \right) \cdot \sin(\alpha) \right]$$

$$T_0 = T_{PWM} - T_1 - T_2$$

where T_{PWM} is the PWM period, and k is the sector number of the command voltage.

In the example shown, the switching sequence is as follows: vector V_3 is on for T_1 seconds, which means that transistor 102 is closed while transistors 104 and 106 remain open. Because transistors 103, 105 and 107 are complimentary to transistors 102, 104 and 106, transistor 103 is open during this period and transistors 105 and 107 are open. Then vector V_2 is applied for T_2 seconds, which corresponds to a state wherein transistor 102 and 106 are closed and transistor 104 is open. Finally zero voltage vector V_8 is applied for T_0 seconds. Voltage vector V_8 corresponds to a state wherein transistors 102, 104 and 106 are all closed. The same result could be achieved by applying voltage vector V_7, which corresponds to a state wherein transistors 102, 104 and 106 are all open,

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1 however vector V_8 is chosen to minimize the number of transistors that must change

2 states.

3   This is one way to implement Space vector PWM. This scheme has the

4 advantage that there are only 4 transitions per PWM cycle and so the switching losses are

5 reduced. However, the disadvantage is that it results in higher current ripple, which

6 results in audible noise. An alternative space vector PWM pattern is shown in Fig. 22a

7 for the same command voltage vector $|V_{cmd}|\angle\alpha_{cmd}$. In this implementation, there are 6

8 switch transitions per PWM cycle thus the current ripple is lower and so there is less

9 noise. This way of implementing space vector PWM splits the time spent on the "zero"

10 voltage vector in half. That is, half of T_0 is spent on vector V_7 and half on vector V_8.

11   B. Advanced Output Control

12   The second group of Inverter DSP control functions relates to advanced UPS

13 output control. The advanced output control functions include controls optimized for

14 load transients and nonlinear loads that produce high crest factor currents. Fig. 26 shows

15 a general inverter structure where the advanced output control method of the present

16 invention may be applied. The goal of the advanced output control is to control the

17 generated PWM voltage (V_{pwm}) in order to regulate the load voltage(s) (V_{load}) under any

18 disturbance caused by the variation of load current(s) (I_{load}), while limiting the inverter

19 current (I_{inv}) to its safest defined level. The control method requires some means of

20 measuring all or part of the voltages and currents that qualify as state variables in a

21 chosen state space model of the output filter and transformer circuit (circuit state

22 variables). Construction of such state space model and selection of the state variables are

23 known to those skilled in the art of control analysis and design. The output control of the

24 present invention may be applied to a single phase, three-phase, or split phase inverter

25 system.

26   The output control method of the present invention uses a two-loop control as

27 shown in Fig. 27. The inner loop regulates the inverter current using a discrete sliding

28 mode controller. This inner current loop provides fast transient response and current

29 limiting for system protection. The outer loop regulates the inverter voltage using a

30 harmonic servomechanism controller. The circuit states variables are used for the

31 construction of both the voltages and current controllers.

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1   The inner discrete sliding mode current control loop provides fast transient

2   response, which is useful to limit current and prevent inverter damage by an overload

3   condition. The discrete sliding mode controller also has zero overshoot, which improves

4   response to load transients.

5   The harmonic servomechanism control improves the critical bus voltage THD by

6   eliminating selected harmonics from the output voltage and provides good output voltage

7   transient performance during load changes. Another advantage of the harmonic

8   servomechanism controller in the present invention is that it is easier to stabilize than

9   similar approaches that use the internal define model principle. One disadvantage of the

10   harmonic servomechanism control is that it can eliminate only a finite number of

11   disturbances in the control model. However, this limitation is not unduly burdensome in

12   practical applications because excellent THD results may be obtained by eliminating only

13   a few critical harmonics.

14   Fig. 28 shows the harmonic servomechanism controller used for the output

15   voltage control. The controller includes servo compensator blocks for the fundamental

16   frequency (Fundamental Servo-Compensator) and the harmonic frequencies to be

17   eliminated (Harmonic Servo-Compensator 2 through n). Each harmonic servo

18   compensator block is driven by the error signal, which is the difference between the

19   reference voltage (V_{ref}) and the actual load voltage (V_{load}). Each compensator block is a

20   state space implementation of the analog transfer function:

21   $$T(s) = \frac{1}{s^2 + \varpi_n^2}$$

22   where $\omega_i = 2\pi \cdot i \cdot f$, f is the fundamental frequency and $i \cdot f$ is the harmonic

23   frequency chosen to be eliminated. Specifically, the following continuous state space

24   implementation of T(s) may be used for each harmonic servo compensator block:

25   $$\dot{\bar{\eta}}_i = \begin{pmatrix} 0 & 1 \\ -\omega_i^2 & 0 \end{pmatrix} \bar{\eta}_i + \begin{pmatrix} 0 \\ 1 \end{pmatrix} e$$

26   This state space form may be further discretized to obtain a discrete state space

27   implementation of the transfer function suitable for digital control implementation. Any

28   standard discretization method known to those skilled in the art may be used for this

29   purpose.

1   The fundamental servo compensator ensures that the actual voltage tracks the
2   reference voltage at the fundamental frequency of 50/60 Hz, while each harmonic servo
3   compensator block ensures the elimination of the corresponding harmonic contents
4   caused by the load disturbances. These conditions are guaranteed by the internal model
5   principle, which states that if frequency modes (poles) of the references and the
6   disturbances to be eliminated are included in the control loop, then the steady state error
7   will not contain these frequency contents. Each of these harmonic compensators can be
8   viewed as a controlled sine wave signal generators running at the specified harmonic
9   frequency. Each controlled signal generator reacts only to the existence of the
10   corresponding harmonic in the error signals and adjusts the inverter current commands to
11   force the corresponding harmonic content of the error to zero.

12   The inverter current command signal generated by the harmonic servomechanism
13   voltage controller is constructed from linear combinations of the states of the servo
14   compensators and the circuit state variables feedback. This is shown in Fig. 28 as the
15   constant gains block $K1$, which multiply the servo compensator states and gains
16   $K2$ which multiply the circuit state variables. The gains $K1$ and $K2$ are chosen to
17   ensure stability of the overall closed loop system and to provide good transient
18   performance.

19   The method of the invention may also include the steps for calculating the gains
20   $K1$ and $K2$ using an optimal state feedback, which may improve the stability and
21   transient response of the control system. The basic theory of using an optimal state
22   feedback for calculating gains $K1$ and $K2$ is known to those skilled in the art as the
23   perfect robust servomechanism control problem as described in Davison, E.J. and
24   Scherzinger, B., "Perfect Control of the robust servomechanism problem", *IEEE Trans.*
25   *On Automatic Control,* 32 (8), 689-702, 1987. Application of this basic theory to the
26   present invention, however, requires certain extensions and modifications, due to the
27   inclusion of the discrete time sliding mode controller in the inner current loop and the
28   inherent delay introduced by digital implementation of the controller. Fig. 29 shows the
29   timing diagram of the PWM gating signals generation in relation with the A/D sampling
30   time of the DSP. It can be seen that there is a one-half PWM period delay between the
31   time the signals are sampled by the A/D and the time the PWM control action is applied.

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1   To best explain the method of the present invention for calculating the control gains, a

2 specific example of a three-phase PWM inverter as in Fig. 30 will be used. The following

3 paragraphs detail the method as applied to the inverter system in Fig. 30.

4   The inverter system in Fig. 30 consists of a three-phase PWM voltage IGBT

5 inverter with LC output filter (L_{inv} and C_{inv}) and a delta-wye transformer that act both as a

6 potential transformer and electrical isolation to the load. Small capacitors (denoted as

7 C_{grass} in Fig. 30) are added at the load side of the transformer to provide further harmonic

8 filtering and stabilization of the load voltages. A DSP (Digital Signal Processor) system

9 controls the operation of the power converter, providing required PWM gating signals to

10 the power devices. Voltages and currents measured by the DSP system for control

11 purposes are shown labeled in Fig. 30. The line-to-neutral load voltages (at points xyz-n

12 in Fig. 30) are denoted as: $V_{load-an}$, $V_{load-bn}$, and $V_{load-cn}$, the load phase currents as: I_{load-a},

13 I_{load-b}, and I_{load-c}, the line-to-line inverter filter capacitor voltages (at points uvw in Fig.

14 30) as: V_{inv-ab}, V_{inv-bc} and V_{inv-ca}, the inverter phase currents as: I_{inv-a}, I_{inv-b}, and I_{inv-c}

15   For development of the control algorithm, a state space model of the system is

16 needed. Each phase of the delta-wye transformer has been modeled as an ideal

17 transformer with leakage inductance L_{trans} and series resistance R_{trans} on the secondary

18 winding as shown in Fig. 31. The secondary transformer currents are denoted as I_{snd-a},

19 I_{snd-b}, and I_{snd-c}. Using the transformer model in Fig. 31, a state space equation of the

20 output filter circuit in Fig. 1 can be written as in equations (1.a)-(1.d):

21
$$\frac{d\vec{V}inv_{abc}}{dt} = \frac{1}{3 \cdot C_{inv}} \vec{I}inv_{abc} - \frac{1}{3 \cdot C_{inv}} Tr_i \cdot \vec{I}snd_{abc} \qquad (1.a)$$

22
$$\frac{d\vec{I}inv_{abc}}{dt} = \frac{1}{L_{inv}} \vec{V}pwm_{abc} - \frac{1}{L_{inv}} \vec{V}inv_{abc} \qquad (1.b)$$

23
$$\frac{d\vec{V}load_{abc}}{dt} = \frac{1}{C_{load}} \vec{I}snd_{abc} - \frac{1}{C_{load}} \vec{I}load_{abc} \qquad (1.c)$$

24
$$\frac{d\vec{I}snd_{abc}}{dt} = -\frac{R_{trans}}{L_{tran}} \vec{I}snd + \frac{1}{L_{tran}} Tr_v \cdot \vec{V}inv_{abc} \qquad (1.d)$$
$$-\frac{1}{L_{tran}} \vec{V}load_{abc}$$

25 where the voltages and currents vectors are defined as in (2).

26 $\vec{V}inv_{abc} = [Vinv_{ab} \quad Vinv_{bc} \quad Vinv_{ca}]^T$

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1 $$\vec{Vload}_{abc} = [Vload_a \quad Vload_b \quad Vload_c]^T,$$

2 $$\vec{Iload}_{abc} = [Iload_a \quad Iload_b \quad Iload_c]^T \quad \vec{Isnd}_{abc} = [Isnd_a \quad Isnd_b \quad Isnd_c]^T,$$

3 $$\vec{Iinv}_{abc} = [Iinv_{ab} \quad Iinv_{bc} \quad Iinv_{ca}]^T$$
$$= [Iinv_a - Iinv_b \quad Iinv_b - Iinv_c \quad Iinv_c - Iinv_a]^T \qquad (2)$$

4 Matrices Tr_i and Tr_v in the equations above denote the currents and voltages

5 transformations of the delta-wye transformer. Denoting the transformer's turn ratio as tr,

6 these matrices are given by (3):

7 $$Tr_i = tr \cdot \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}, \qquad Tr_v = tr \cdot \begin{bmatrix} 0 & 0 & -1 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \quad (3)$$

8 To obtain a state space model of the system, the dynamic equations in (1) are

9 transformed to the DQ0 stationary reference frame using the transformation:

10 $$\vec{f}_{qd0} = K_S \cdot \vec{f}_{abc}, \qquad (4)$$

11 with

12 $$K_S = \frac{2}{3} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & -\sqrt{3}/2 & \sqrt{3}/2 \\ 0.5 & 0.5 & 0.5 \end{bmatrix},$$

13 $$f_{qd0} = [f_q, f_d, f_0]^T, f_{abc} = [f_a, f_b, f_c]^T$$

14 where $\vec{f}_{abc}$ denotes the abc voltages and currents defined in (2), and $\vec{f}_{qd0}$ the

15 corresponding DQ0 stationary reference frame variables. The circuit dynamics can then

16 be written as in (5.a − 5.d):

17 $$\frac{d\vec{Vinv}_{qd}}{dt} = \frac{1}{3 \cdot C_{inv}} \vec{Iinv}_{qd} - \frac{1}{3 \cdot C_{inv}} Tri_{qd0} \cdot \vec{Isnd}_{qd0} \quad (5.a)$$

18 $$\frac{d\vec{Iinv}_{qd}}{dt} = \frac{1}{L_{inv}} \vec{Vpwm}_{qd} - \frac{1}{L_{inv}} \vec{Vinv}_{qd} \quad (5.b)$$

19 $$\frac{d\vec{Vload}_{qd0}}{dt} = \frac{1}{C_{load}} \vec{Isnd}_{qd0} - \frac{1}{C_{load}} \vec{Iload}_{qd0} \quad (5.c)$$

20 $$\frac{d\vec{Isnd}_{qd0}}{dt} = -\frac{R_{tran}}{L_{tran}} \vec{Isnd}_{qd0} + \frac{1}{L_{tran}} Trv_{qd} \cdot \vec{Vinv}_{qd}$$
$$- \frac{1}{L_{tran}} \vec{Vload}_{qd0} \qquad (5.d)$$

21 where the matrices Tri_{qd0} and Trv_{qd} are defined as:

$$Tri_{qd0} = \left[K_s \cdot Tr_i \cdot K_S^{-1}\right]_{row\,1,2} = tr \cdot \frac{3}{2}\begin{bmatrix} 1 & \sqrt{3} & 0 \\ -\sqrt{3} & 1 & 0 \end{bmatrix} \quad (6.\text{a})$$

$$Trv_{qd} = \left[K_s \cdot Tr_v \cdot K_S^{-1}\right]_{col\,1,2} = tr \cdot \frac{1}{2}\begin{bmatrix} 1 & -\sqrt{3} \\ \sqrt{3} & 1 \\ 0 & 0 \end{bmatrix} \quad (6.\text{b})$$

Notice that, due to the three-wire system of the inverter and filter, the zero components of the inverter voltages ($\vec{V}inv_{qd}$), the inverter currents ($\vec{I}inv_{qd}$) and the input PWM voltages $\vec{V}pwm_{qd}$ are trivial and they do not appear in the equations above.

The next two subsections summarize the development of the two control loops, the inner current loop using the discrete sliding mode controller and the voltage control loop using the robust servomechanism principles. For designing the discrete time sliding mode current controller, consider the inverter and filter subsystem with no transformer and load dynamics:

$$\frac{d\vec{V}inv_{qd}}{dt} = \frac{1}{3 \cdot C_{inv}}\vec{I}inv_{qd} - \frac{1}{3 \cdot C_{inv}}Tri_{qd0} \cdot \vec{I}snd_{qd0} \quad (24.\text{a})$$

$$\frac{d\vec{I}inv_{qd}}{dt} = \frac{1}{L_{inv}}\vec{V}pwm_{qd} - \frac{1}{L_{inv}}\vec{V}inv_{qd} \quad (24.\text{b})$$

Assuming the secondary transformer currents $\vec{I}snd_{qd0}$ as disturbances, this subsystem can be written in state space form as:

$$\dot{\vec{x}}_1 = A_1\vec{x}_1 + B_1\vec{u} + E_1\vec{d}_1 \quad (25)$$

$$\vec{A}_1 = \begin{bmatrix} \bar{0}_{2x2} & (3 \cdot C_{inv})^{-1} \cdot \vec{I}_{2x2} \\ -(L_{inv})^{-1} \cdot \vec{I}_{2x2} & \bar{0}_{2x2} \end{bmatrix}, \quad \vec{B}_1 = \begin{bmatrix} \bar{0}_{2x2} \\ (L_{inv})^{-1} \cdot \vec{I}_{2x2} \end{bmatrix}, \quad \vec{E}_1 = \begin{bmatrix} -(3 \cdot C_{inv})^{-1} \cdot Tri_{qd0} \\ \bar{0}_{2x3} \end{bmatrix},$$

where the states are $\vec{x}_1 = \left[\vec{V}inv_{qd}, \vec{I}inv_{qd}\right]$, the inputs $\vec{u} = \vec{V}pwm_{qd}$ and disturbances $\vec{d}_1 = \vec{I}snd_{qd}$.

The discrete form of (25) can be calculated as:

$$\vec{x}_1(k+1) = A_1^*\vec{x}_1(k) + B_1^*\vec{u}(k) + E_1^*\vec{d}_1(k)$$

where

$$A_1^* = \exp(A \cdot T_S) \quad B_1^* = \int_0^{T_s} e^{A_1 \cdot Ts} B_1\,d\tau$$

$$E_1^* = \int_0^{T_s} e^{A_1 \cdot Ts} E_1\,d\tau$$

and T_S is the A/D sampling time, which in this case is equal to the PWM period T_{pwm}

To force the inverter currents to follow their commands, the sliding mode surface is chosen as: $\bar{s}(k) = C_1 \cdot \bar{x}_1(k) - \bar{I}cmd(k)$ where $C_1 \cdot \bar{x}_1(k) = \bar{I}inv_{qd}(k)$, so that when discrete sliding mode occurs, we have $\bar{s}(k) = 0$ or $\bar{I}inv(k) = \bar{I}cmd(k)$. The existence of the discrete sliding mode can be guaranteed if the control is given:

$$u(k) = \begin{cases} \bar{u}_{eq}(k) & \text{for} \quad \left\| \bar{u}_{eq}(k) \right\| \leq u_0 \\ u_0 \dfrac{\bar{u}_{eq}(k)}{\left\| \bar{u}_{eq}(k) \right\|} & \text{for} \quad \left\| \bar{u}_{eq}(k) \right\| > u_0 \end{cases} \qquad (26)$$

where the equivalent control input $\bar{u}_{eq}(k)$ is calculated from:

$$\bar{u}_{eq}(k) = \left(C_1 B_1^* \right)^{-1} \left(\bar{I}cmd_{qd} - C_1 A_1^* \bar{x}_1(k) - C_1 E_1^* \bar{d}_1(k) \right) \qquad (27)$$

and u_0 denotes the maximum value of the PWM voltage command realizable by the space vector algorithm.

Note that the secondary transformer currents are needed for the control, but these currents are not measured in the system (see Fig. 31). A linear Luenberger observer can be easily designed to estimate these currents for control purposes. However, in most practical cases we can approximate these currents with the load currents (*i.e.* $\bar{I}snd_{qd} \approx \bar{I}load_{qd}$), because the currents through the output capacitor filters are small. According to the inventors' experience, the effect of using this approximation is unnoticeable in the control performance.

Due to the computation delay of the DSP, the control action given by above will result in undesirable overshoots during transients. This effect can be minimized, however, if the states $\bar{x}_1(k)$ and disturbances $\bar{d}_1(k)$ are replaced with their first order one-half step ahead predicted values given by:

$$\bar{x}_1^P(k) = 1.5 \cdot \bar{x}_1(k) - 0.5 \cdot \bar{x}_1(k-1)$$

$$\bar{d}_1^P(k) = 1.5 \cdot \bar{d}_1(k) - 0.5 \cdot \bar{d}_1(k-1) \qquad (28)$$

The equivalent control input $\bar{u}_{eq}(k)$ then becomes:

$$\bar{u}_{eq}(k) = \left(C_1 B_1^* \right)^{-1} \left(\bar{I}cmd_{qd} - C_1 A_1^* \bar{x}_1^P(k) - C_1 E_1^* \bar{d}_1^P(k) \right) \qquad (29)$$

1   The voltage control loop designed in this invention is based on the discrete form

2 of the technique developed in Davison, cited above. To design the load voltages

3 controller, first consider the entire plant system with the-0 components of the voltages

4 and currents omitted as given above. As explained earlier, these 0-components are

5 completely decoupled and uncontrollable from the inputs, and therefore are not useful to

6 be included in the design. In the system, an input delay of one-half the PWM period

7 ($0.5T_{pwm}$) has been explicitly included to account for the computation delay of the DSP.

8
$$\dot{\vec{x}}_p(t) = A_p \vec{x}_p(t) + B_p \vec{u}(t - 0.5T_{pwm}),$$

9
$$\bar{A}_p = \begin{bmatrix} \bar{0}_{2x2} & (3 \cdot C_{inv})^{-1} \cdot \bar{I}_{2x2} & \bar{0}_{2x2} & -(3 \cdot C_{inv})^{-1} \cdot \hat{Tr}_{iqd} \\ -(L_{inv})^{-1} \cdot \bar{I}_{2x2} & \bar{0}_{2x2} & \bar{0}_{2x2} & \bar{0}_{2x2} \\ \bar{0}_{2x2} & \bar{0}_{2x2} & \bar{0}_{2x2} & (C_{load})^{-1} \cdot \bar{I}_{2x2} \\ (L_{inv})^{-1} \cdot \hat{Tr}_{vqd} & \bar{0}_{2x2} & -(L_{inv})^{-1} \cdot \bar{I}_{2x2} & -R_{trans}(L_{trans})^{-1} \cdot \bar{I}_{2x2} \end{bmatrix},$$

10
$$\bar{B}_p = \begin{bmatrix} \bar{0}_{2x2} \\ (L_{inv})^{-1} \cdot \bar{I}_{2x2} \\ \bar{0}_{2x2} \\ \bar{0}_{2x2} \end{bmatrix}, \quad \hat{Tr}_{iqd} = tr \cdot \frac{3}{2}\begin{bmatrix} 1 & \sqrt{3} \\ -\sqrt{3} & 1 \end{bmatrix} \quad \hat{Tr}_{vqd} = tr \cdot \frac{1}{2}\begin{bmatrix} 1 & -\sqrt{3} \\ \sqrt{3} & 1 \end{bmatrix} \quad (30)$$

11   The states variables for the system (30) are chosen as

12 $\vec{x}_p = [\vec{V}inv_{qd}, \vec{I}inv_{qd}, \vec{V}load_{qd}, \vec{I}snd_{qd}]$, with the inputs as $u = \vec{V}pwm_{qd}$. System (30) can be

13 transformed to a discrete-time system with sampling time $T_s = T_{pwm}$ to yield:

14
$$\vec{x}_p(k+1) = \Phi \cdot \vec{x}_p(k) + \Gamma_1 \cdot \vec{u}(k-1) + \Gamma_2 \cdot \vec{u}(k) \qquad (31)$$

15 where

16
$$\Phi = e^{A_p T_s}, \quad \Gamma_1 = \int_{0.5T_s}^{T_s} e^{A_p \tau} B_p d\tau, \quad \Gamma_2 = \int_0^{0.5T_s} e^{A_p \tau} B_p d\tau$$

17   Discrete time system (31) can be written in a standard discrete time state space

18 equations by adding the extra states: $\vec{x}_a(k) = \vec{u}(k-1) = \vec{V}pwm_{qd}(k-1)$ to yield:

19
$$\begin{bmatrix} \vec{x}_p(k+1) \\ \vec{x}_a(k+1) \end{bmatrix} = \begin{bmatrix} \Phi & \Gamma_1 \\ \bar{0}_{2x2} & \bar{0}_{2x2} \end{bmatrix} \cdot \begin{bmatrix} \vec{x}_p(k) \\ \vec{x}_a(k) \end{bmatrix} + \begin{bmatrix} \Gamma_2 \\ \bar{I}_{2x2} \end{bmatrix} \cdot \vec{u}(k) \qquad (32)$$

20 so that the system can be written as:

21
$$\vec{x}_p^*(k+1) = A_p^* \vec{x}_p^*(k) + B_p^* \vec{u}(k) \qquad (33)$$

22 where:

1 $$\vec{x}_p^*(k)=\begin{bmatrix}\vec{x}_p(k)\\ \vec{x}_a(k)\end{bmatrix}, \quad A_p^*=\begin{bmatrix}\Phi & \Gamma_1\\ \vec{0}_{2x2} & \vec{0}_{2x2}\end{bmatrix}, \quad B_p^*=\begin{bmatrix}\Gamma_2\\ \vec{I}_{2x2}\end{bmatrix}$$

2 To design the voltage controller, we need to consider the true plant (33) and the

3 discrete time sliding mode current controller as the equivalent 'plant' as seen by the outer

4 voltage loop. Using equation (27) and (33) the augmented true plant and discrete sliding

5 mode current controller can be found as in (34).

6 $$\vec{x}_p^*(k+1)=A_d\vec{x}_p^*(k)+B_d\vec{u}_1(k) \qquad (34)$$

7 with $\vec{u}_1(k)=\vec{I}cmd_{qd}^*(k)$, and

8 $$A_d=A_p^*-B_p^*\left(C_1B_1^*\right)^{-1}\left(B_1^*C_{11}+E_1^*C_{12}\right)$$

9 $$B_d=B_p^*\left(C_1B_1^*\right)^{-1}$$

10 $$C_{11}=\begin{bmatrix}\vec{I}_{2x2} & \vec{0}_{2x2} & \vec{0}_{2x2} & \vec{0}_{2x2} & \vec{0}_{2x2}\\ \vec{0}_{2x2} & \vec{I}_{2x2} & \vec{0}_{2x2} & \vec{0}_{2x2} & \vec{0}_{2x2}\end{bmatrix}$$

11 $$C_{12}=\begin{bmatrix}\vec{0}_{2x2} & \vec{0}_{2x2} & \vec{0}_{2x2} & \vec{I}_{2x2} & \vec{0}_{2x2}\end{bmatrix}$$

12 Note that the augmented system given in (34) was found assuming the

13 approximation $\vec{I}snd_{qd} \approx \vec{I}load_{qd}$ has been used.

14 Now, assume $\omega_i=2\pi f_i \quad i=1,2,...n$ are frequencies of the reference voltages and

15 harmonics to be eliminated. For a 60-Hz UPS system with desire to eliminate 5th and 7th

16 harmonics, for example, we use $\omega_1=2\pi\cdot60$, $\omega_2=2\pi\cdot5\cdot60$, and $\omega_3=2\pi\cdot7\cdot60$. We can

17 then choose the servo-compensator to be of the form (35):

18 $$\dot{\vec{\eta}}=A_c\vec{\eta}+B_ce_{Vqd}$$

19 $$e_{Vqd}=\vec{V}ref_{qd}-\vec{V}load_{qd} \qquad (35)$$

20 where

21 $$\vec{\eta}=[\vec{\eta}_1,\vec{\eta}_2,\cdots\vec{\eta}_n]^T \qquad \vec{\eta}_i\in R^4, \quad i=1,2,...n$$

22 $$A_c=\text{block diag}[Ac_1,Ac_2,\cdots,Ac_n]$$

23 $$B_c=[Bc_1,Bc_2,\cdots,Bc_n]^T$$

24 with

25 $$Ac_i=\begin{pmatrix}\vec{0}_{2x2} & \vec{I}_{2x2}\\ -\omega_i^2\vec{I}_{2x2} & \vec{0}_{2x2}\end{pmatrix}, \quad i=1,2,...n$$

1    $Bc_i = \begin{pmatrix} \bar{0}_{2x2} & \bar{I}_{2x2} \end{pmatrix}^T$ $i = 1, 2, \ldots n$

2   Note that each of the blocks $\dot{\bar{\eta}}_i = Ac_i\bar{\eta}_i + Bc_i\bar{e}_{Vqd}$ represents a state space

3   implementation of the continuous transfer function: $1/\left(s^2 + \omega_i^2\right)$ for each of the qd-axis

4   voltages errors.

5   The servo compensator (35) can be transformed to a discrete time system to yield:

6    $\bar{\eta}(k+1) = A_c^*\bar{\eta}(k) + B_c^*\bar{e}_{Vqd}(k)$, $\bar{e}_{Vqd}(k) = \bar{V}ref_{qd}(k) - \bar{V}load_{qd}(k)$ (36)

7   where:

8    $A_c^* = \exp(A_c \cdot T_S)$ $B_c^* = \int_0^{T_S} e^{A_1 \cdot (T_s - \tau)} B_c \, d\tau$

9   Now that we have determined the 'plant' and the servo compensator, the control

10   input for the perfect robust servomechanism controller is given by:

11    $\bar{u}_1(k) = \bar{I}cmd_{qd}^*(k) = K_0 x_p^*(k) + K_1\eta(k)$ (37)

12   where the gains $K = \begin{bmatrix} K_0 & K_1 \end{bmatrix}$ are found by minimizing the discrete performance

13   index:

14    $J_\varepsilon = \sum_{k=0}^{\infty}\left(z(k)'z(k) + \varepsilon \cdot u(k)'u(k)\right)$,

15    $z = \begin{bmatrix} x_p^* \\ \eta \end{bmatrix}$ (38)

16   for the augmented 'equivalent plant' (34) and the servo compensator (36):

17    $\begin{bmatrix} \bar{x}_p^*(k+1) \\ \eta(k+1) \end{bmatrix} = \begin{bmatrix} A_d & 0 \\ -B_c^*C & A_c^* \end{bmatrix}\begin{bmatrix} \bar{x}_p^*(k) \\ \eta(k) \end{bmatrix} + \begin{bmatrix} B_d \\ -B_c^*D \end{bmatrix}u_1(k)$ (39)

18   where $\varepsilon > 0$ is an arbitrarily small scalar.

19   The current command $\bar{I}cmd_{qd}^*(k)$ generated by the robust servomechanism voltage

20   controller above is limited in magnitude as in (40) to yield the current command

21    $\bar{I}cmd_{qd}(k)$, which will be implemented by the inner loop current controller:

22    $\bar{I}cmd_{qd}(k) = \begin{cases} \bar{I}cmd_{qd}^*(k) & \text{if } \left|\bar{I}cmd_{qd}^*(k)\right| \leq I_{\max} \\ \dfrac{\bar{I}cmd_{qd}^*(k)}{\left|\bar{I}cmd_{qd}^*(k)\right|}I_{\max} & \text{if } \left|\bar{I}cmd_{qd}^*(k)\right| > I_{\max} \end{cases}$ (40)

I_{max} represents the maximum allowable magnitude of the inverter currents. Equation (40) limits the magnitude of the current commands but maintains their vector directions in the qd-space.

The states $\bar{\eta}_i$ of the servo-compensator can be seen as sine wave signal generators that get excited by the harmonic contents of the error signals at frequency ω_i. When the control inputs of the robust servomechanism voltage controller saturate i.e., $\left|\bar{I}cmd_{qd}^*(k)\right| > I_{max}$ the servo-compensator states will grow in magnitude due to the break in the control loop. This problem is similar to the integrator windup problem that occurs in an integral type controller. To prevent this, the servo-compensator in (36) can be modified as follows:

$$\bar{\eta}(k+1) = A_c^* \bar{\eta}(k) + B_c^* \bar{e}_1(k),$$

$$\bar{e}_1(k) = \begin{cases} \bar{e}_{Vqd}(k) & \text{if } \left|\bar{I}cmd_{qd}^*\right| \leq I_{max} \\ 0 & \text{if } \left|\bar{I}cmd_{qd}^*\right| > I_{max} \end{cases} \qquad (41)$$

Using (41), during the current limit saturation, the servo compensator states will continue to oscillate at the harmonic frequency with constant magnitude. The resulting discrete servomechanism controller structure is shown in Fig. 32 and Fig. 33

C. PLL Features

The third group of Inverter DSP control functions relates to bypass static switch control, PLL control, and detecting abnormal operations. This group of functions monitors system measurements, both digital and analog, and makes decisions as to whether or not the inverter can safely support the load or is supporting the load adequately. If, for some reason, the inverter cannot or is not supporting the load, these functions notify the inverter DSP system of the problem.

The inverter DSP has 2 PLLs, one that locks to the bypass voltage and another that synchronizes the inverter voltage to the bypass voltage. The PLL that tracks the bypass voltage is the same PLL that uses DQ transformation as described above. The second PLL operates differently because the inverter's output frequency is not allowed to change rapidly. The seconds PLL's operation is described below.

The rate of change of frequency is referred to as a slew rate. This slew rate is limited by the inverter DSP because some loads are sensitive to frequency variations.

1   This limit can pose a problem when trying to phase lock to an external source (like the

2 bypass source). The basic PLL algorithm operates by determining the difference between

3 the bypass phase angle and the inverter phase angle. If the difference is positive then the

4 inverter frequency is increased so that the inverter phase angle catches up to the bypass

5 phase angle. If the phase angle difference is negative, then the inverter frequency is

6 decreased so that the bypass phase catches up to the inverter phase.

7   When the frequency slew rate is limited, the bypass phase angle will repeatedly

8 pass the inverter phase angle. This happens because half the time the phase difference is

9 positive and the other half of the time the phase difference is negative and so the inverter

10 increases the frequency half the time and then decreases the frequency half the time thus

11 it never catches up to the external source.

12   In the UPS of the present invention, this basic algorithm is modified such that the

13 frequency difference is minimized first, then the phase difference is minimized. The

14 modified algorithm works as follows. If the frequency difference between the bypass and

15 inverter is positive, then the inverter frequency is increased but not by an amount greater

16 than the maximum slew rate. When the absolute value of the frequency difference is

17 within some predetermined range, the inverter's frequency is held constant. The absolute

18 value of phase angle difference is then tracked and when it is within some predetermined

19 range, the inverter frequency is again increased (or decreased as appropriate) to further

20 reduce the frequency difference. When the absolute value of the frequency difference is

21 within a second predetermined range, it is again held constant and the phase angle

22 difference is allowed to decrease until the phase angle difference is within some second

23 predetermined range. This process continues until both the frequency difference and

24 phase angle difference is within some arbitrarily small range at which time the inverter's

25 frequency and phase angle is set equal to the bypass's frequency and phase angle.

26   D. Transfer Features

27   A fourth group of Inverter DSP control functions are the transfer control

28 functions, which are used when the UPS transfers from the normal inverter power source

29 to the bypass power source or from bypass power to inverter power. Transfers between

30 the power sources can be done manually via the different user interfaces or the UPS

31 control board can automatically perform the transfers. An automatic transfer from the

1   inverter source to the bypass source occurs if the UPS control decides that the inverter

2   cannot continue to support the load. An automatic transfer from bypass source to inverter

3   source occurs when the inverter DSP detects that all systems are functioning correctly

4   and the load was previously automatically transferred to the bypass.

5   During a transfer from bypass power to inverter power, the outer voltage control

6   loop regulates the inverter voltage (the voltage at the primary side of output transformer).

7   The outer voltage control loop matches the bypass phase using information from the PLL.

8   It matches the bypass magnitude, provided that the bypass is qualified. First, the output

9   contactor is closed, putting the inverter and bypass in parallel. Next the inverter angle is

10 adjusted so that it is leading with respect to the bypass. This causes the inverter to

11 acquire the output load from the bypass. When the inverter has acquired the load, for

12 example, it has 93% of the load, the bypass is turned off. A one-line cycle delay is

13 initiated to allow the bypass to fully commutate off. After this delay, the outer voltage

14 control loop switches to regulating the output voltage (the voltage at the secondary side

15 of the output transformer). If the bypass is not qualified or the inverter and bypass are

16 not properly synchronized, then the transfer to inverter does not occur.

17   There are two situations in which the inverter will transfer from inverter power to

18 bypass power, normal transfer, also called manual transfer, and emergency transfer, also

19 called automatic transfer, as mentioned above. An emergency transfer occurs when a

20 fault is detected by the inverter DSP. If the bypass is qualified and the inverter and

21 bypass are properly synchronized, then the bypass is turned on immediately. Next, the

22 inverter is turned off, and finally the output contactor is opened. If the bypass and

23 inverter are not synchronized, then the bypass is not turned on until the output contactor

24 is opened. The unsynchronized transfer is called an interrupted transfer because the

25 output load will be dropped momentarily (100 milliseconds or more) before the bypass

26 re-energized the output. If the bypass is not qualified, then the inverter simply turns off

27 and opens the output contactor, dropping the load.

28   For a normal transfer to bypass, the inverter first switches from controlling the

29 output voltage to controlling the inverter voltage. The inverter voltage is matched to the

30 bypass voltage phase and magnitude. A 5-cycle delay allows the control to switch into

31 this mode. After the delay, the bypass is turned on and the output contactor is opened.

1   The inverter keeps running, but the load has been transferred to the bypass seamlessly.

2   Again, if the inverter and bypass are not synchronized, the output contactor will open

3   before the bypass is energized (an interrupted transfer). Likewise if the bypass is not

4   qualified, then the output load will be dropped.

5   The bypass source can also be paralleled with the inverter source in the event of a

6   large transient overload at the output. This mode is called Pulse Parallel. In this mode,

7   when the inverter DSP detects a large overload situation (like 250% or more), the control

8   will turn-on the bypass switch, provided the bypass source is qualified and properly

9   synchronized with the inverter. The inverter switches from controlling the output voltage

10   to controlling the inverter voltage, but the output contactor stays closed, thus both sources

11   are supporting the load. The inverter's current limit is reduced to protect it from the large

12   overload. After a number of line-cycles (about 10), the bypass switch will be turned off

13   if the overload has cleared. The inverter will switch to controlling the output voltage

14   after a 1 line-cycle delay. If the overload remains, then the output contactor will be

15   opened thus isolating the inverter from the overload. Pulse Parallel mode allows for the

16   UPS to safely handle large overloads that only last for a short period of time. Loads that

17   have such characteristic are motors starting, transformers energizing and energizing high

18   crest factor loads.

19   E. Parallel Operation

20   The fifth group of control functions implemented by the Inverter DSP relates to

21   controlling multiple UPS units in parallel. Parallel operation of multiple UPS units may

22   be done for additional capacity or redundancy. To allow parallel operation, the Inverter

23   DSP performs PLL sharing, load sharing, inverter synchronization, and load bus

24   synchronization among the parallel-connected units. Digital load sharing control requires

25   adaptive tuning to eliminate power mismatches among the parallel-connected units. The

26   Inverter DSP can control parallel-connected units in 1+N mode, central mode, or load bus

27   sync mode. Current imbalance between the paralleled units is eliminated by relative

28   phase adjustment of the voltage supplied by each unit. The voltage supplied by each unit

29   is adjusted to produce equal current sharing among the parallel connected units. A phase

30   angle adjustment of the fundamental voltage reference shifts the real power supplied at a

1   fundamental frequency, while an amplitude adjustment changes the fundamental
2   frequency reactive power balance.

3   In addition to this, the present invention includes a method of enforcing harmonic
4   current sharing for those harmonics included in the harmonic servomechanism voltage
5   control. This is achieved by shifting the locations of the harmonic servo compensator
6   poles based on the level of the harmonic distortion of the load currents at the
7   corresponding harmonic frequencies. The poles are moved such that the gain and
8   bandwidth of the control affecting each harmonic is reduced in the presence of the
9   corresponding harmonic in the load current. This effectively builds in an output
10   impedance for that harmonic component of the load currents, which encourages the
11   separate modules to share the current harmonics.

12   The principle of gain (and bandwidth) reduction of the voltage loop in the
13   presence of distortion components for harmonic sharing is commonly known as harmonic
14   drooping. The harmonic drooping method of the present invention has an advantage over
15   the prior art in that because the droop only affects the control gain (bandwidth) of each
16   individual harmonic in the harmonic servo compensator, without affecting the
17   fundamental one. Prior art controllers perform harmonic drooping by reducing the
18   overall gain of the voltage loop based on the total harmonic distortion of the load current,
19   which is undesirable because this will degrade the regulation and transient performance
20   of the fundamental component of the output voltage control. This fact presents yet
21   another advantage of using the harmonic servomechanism controller as the outer voltage
22   loop in the present invention.

23   F.   Adaptive Overload Compensation

24   Digital control of the inverter allows adaptive overload compensation. In general
25   the overload control logic operates as follows. While running on inverter power in an
26   overload situation, a timer is started and set to time out when the thermal capacity of the
27   inverter or magnetic components is reached. The thermal capacity of the UPS is
28   determined empirically, and a sample overload curve is illustrated in Fig. 23.

29   Turning to Fig. 23, the overload rating of a typical UPS is illustrated. The time in
30   an overload condition is plotted along the horizontal axis. The percentage of UPS
31   capacity is plotted along the vertical axis. The blocked in areas illustrate the observed

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1   data, and the dashed line illustrates an approximation curve programmed into the UPS
2   controller. For example, the UPS can maintain a 150% load for approximately 60
3   seconds, but can maintain a 125% load for approximately 600 seconds.

4   From the overload curve an equivalent energy curve may be derived, which
5   represents the total amount of energy that is absorbed by the UPS heat sinks during an
6   overload. This energy must be dissipated after the overload condition is removed before
7   the inverter can support the load again. The time period from the end of the overload
8   until the load can safely be returned to the inverter is defined as the unwind time. A
9   sample equivalent energy curve derived from the overload curve in Fig. 23 is illustrated
10   in Fig. 24.

11   The digital control of the UPS allows a variable unwind rate. For low total energy
12   overloads, the UPS can unwind very quickly. The peak energy for this sample overload
13   curve, Fit. 23, occurs at 125% as shown in Fig. 24. Note that less total energy is
14   absorbed by overloads either greater than 125% or less than 125%. This adaptive
15   determination of the required unwind time allows the UPS to return to inverter operation
16   as quickly as possible, while still protecting the UPS components from thermal damage.

17   The adaptive unwind operation is as follows. When the overload begins, a timer
18   is started which times out at the thermal capacity of the unit for the given load condition,
19   see Fig. 23, for example. The UPS measures the energy into the heat sink indirectly by
20   measuring the UPS kVA, power (kW) and current, as well as the time that the load is
21   applied. The controller uses continuous measurements of the kVA, power, and current to
22   determine an average overload. The UPS controller correlates these measurements to the
23   empirical values discussed above. There is no need to measure the actual heat sink
24   temperature. When the thermal capacity is exceeded, the UPS switches to bypass
25   operation and computes the required unwind time. An unwind timer starts counting
26   down, and when it reaches zero, the load can be safely supported by the inverter again.

27   The adaptive overload system can also compensate for intermittent non-
28   continuous overloads. When the unit is overloaded, the unit operates as described above.
29   If the overload condition corrects itself and the load returns to normal, the controller
30   begins the unwind countdown. If another overload condition occurs before the unwind
31   cycle is completed the new overload energy is added to the remaining overload energy

1   that has not yet dissipated. This cycle may repeat several times, but each time the energy

2   absorbed by the heat sink is tracked, and if it exceeds the limit, the load will be

3   transferred to the bypass, hence this algorithm provides better overload protection for the

4   UPS. This overload algorithm is also applied to the bypass source, but with a different

5   overload curve.

6   G. Transistor Saturation Detection

7   Another novel aspect of the UPS of the present invention is the circuitry and

8   technique for detection of current saturation of the inverter transistors. Transistor current

9   saturation is undesirable in that it will cause catastrophic failure of the transistors as well

10   as a short circuit of the DC bus. It is therefore desirable to shut off the transistors if

11   saturation is detected. Prior art saturation detection techniques monitored the voltage

12   between the transistor collector and emitter (for bipolar junction transistors or BJTs) or

13   between the drain and source (for field effect transistors or FETs) to detect transistor

14   saturation. The problem with detecting saturation using the voltage across the transistor

15   is that the on-voltage across the transistor is typically very small, and the saturation

16   voltage is very difficult to accurately detect.

17   The present invention uses a novel saturation detection technique in which

18   saturation is detected by monitoring the peak current out of the DC bus capacitor. This

19   method is particularly advantageous for use with a UPS controlled by DSPs as opposed to

20   conventional analog control circuits. The transistor saturation detection circuitry may be

21   better understood with reference to Fig. 18. Fig. 18A illustrates a simplified diagram of a

22   single phase inverter. The inverter comprises input DC bus 1800, which further

23   comprises positive DC rail 1801 and negative DC rail 1802. DC bus capacitor 1810 is

24   disposed between the positive and negative DC rails, i.e., across DC bus 1800. The

25   inverter also comprises output AC bus 1803, comprising first and second rails 1804 and

26   1805, respectively. Finally, the inverter also comprises switching transistors 1806, 1807,

27   1808, and 1809.

28   In accordance with the present invention, saturation of the switching transistors is

29   detected by measuring the current through DC bus capacitor 1810. Therefore current

30   transformer ("CT") 1811 is disposed about a lead of said capacitor. CT 1811 is hard

31   wired into the Inverter DSP. If a sufficiently large current is detected flowing through

1   capacitor 1810 by CT 1811, the gate signals to switching transistors 1806, 1807, 1808,

2   and 1809 are all turned off. The direct hardware link to the transistor driver circuits shuts

3   off all transistors by shutting off the gate drive circuits.

4   Sensing the capacitor current may be used to determine when one or more of the

5   switching transistors have failed, causing a short across the DC bus, or when a misfire of

6   one or more switching transistors causes a short across the DC bus. The voltage

7   generated by CT 1811 passes through peak detection circuit illustrated in Fig. 18B, which

8   generates the signal illustrated. As noted above, the UPS controller will shut off all the

9   transistors if the I_DC_PEAK signal is detected.

10   The I_DC_PEAK signal is filtered by the low pass filter circuit illustrated in Fig.

11 18C. The filtered output signal is identified as I_DC_PEAK_FLT'. The filtered signal

12 is AND'ed with the signal IGBT_CRV_FLT to create the signal IGBT_FLT'. This

13 signal is then input into the Inverter DSP, which turns off the IGBT drive signals via a

14 hardwired circuit internal to the DSP. The I_DC_PEAK_FLT may also be used as a

15 digital input that allows determination what caused an inverter shutdown.

16   A principal benefit of the transistor saturation detection circuitry is increased

17 reliability at a reduced cost. Prior art saturation detection circuitry is required for every

18 device (transistor). Conversely, the disclosed transistor saturation detection circuitry

19 monitors and protects all devices with a single circuit. Thus, the system of the present

20 invention results in increased reliability at a reduced cost, because of the simplicity of the

21 invention.

22   H. Miscellaneous

23   The sixth group of Inverter DSP control functions are for processor input and

24 output control, which includes analog input multiplexer setup, analog to digital converter

25 reading, storing the analog input values in memory, calibrating and scaling the stored

26 values, saving the instantaneous analog input values in the proper memories, storing the

27 computed RMS values in the RMS array, reading the digital input port values, updating

28 the corresponding variables, and writing to the digital output port.

REFERENCES

The following references, to the extent that they provide exemplary procedural or other details supplementary to those set forth herein, are specifically incorporated herein by reference.

Copending non-provisional patent application serial number 09/783,273, entitled "Digital Cotnrol of Voltage Harmonic Distortion and Overload Current Protection for Inverters", filed February 13, 2001.

Provisional U.S. Application serial number 60/244,005, entitled "Uninterruptible Power Supply", filed October 27, 2000.

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